Digital technology roadmap

Electrical and digital simulation & verification using educational boards and laboratories

Quartus Prime / ispLEVER Classic, Diamond / ISE, Vivado

ModelSim / Active HDL / ISim

Large volume of production

Verilog, VHDL & System C

Systems on Chip (SoC) & ASICS (GA)

Intel/Lattice/Xilinx FPGA

(>100k logic gates)

Systems on Programmable Chip **(SoPC)**

Professional applications in Telecommunications Systems and Networks

Intel/Lattice/AMD CPLD and **FPGA**

(2,5k – 100k logic gates)

Chapter 3: Microcontrollers (µC)

PIC18F /16F / ATmega **families of microcontrollers**

Integrated development environment tools (MPLABX, XC8 compiler, **C language**, **simulation Proteus-VSM**)

Schematics

&

VHDL

The versatile sPLD 22V10

(~500 logic gates)

Chapter 2: Sequential systems and FSM

Dedicated processors
(Datapath + control unit)

subsystems and peripherals

PROTEUS VSM

Theory and examples from classic 74 TTL and CMOS

(SSI & MSI)

Introductory circuits & FSM

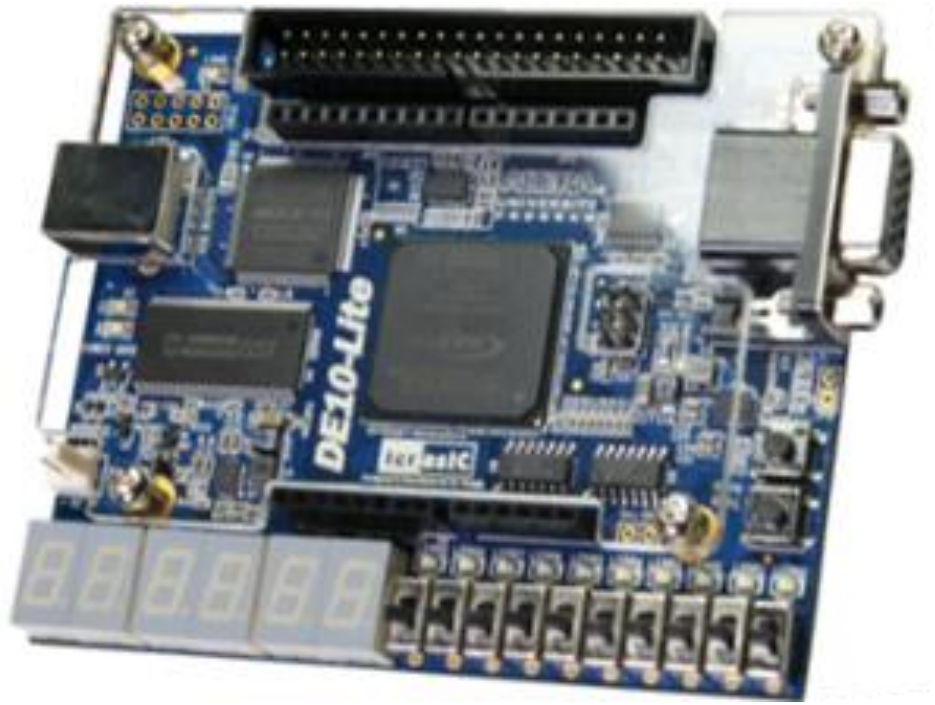
Chapter 1: Combinational circuits

Digital Circuits & Systems

Advanced optional subjects or research

Lab training boards and target chips

Intel/Lattice/AMD FPGA



Microchip PIC18F

Chapter 1: Combinational circuits → **Chapter 2: Sequential systems and FSM (Finite State Machines)** → **Chapter 3: Microcontrollers (µC)**

CSD competencies

- Programmable logic devices and VHDL
- Microcontrollers and C
- Lab skills

- Team work
- Self-directed learning
- Project management (time and due date)
- English
- Oral and written communication
- (UPC email address)

Learning goal:

Using cross-curricular competences and PBL methodology, let us systematically analyse, design, simulate, implement, report, present and reflect about digital circuits and systems using state-of-the-art programmable devices, CAD/EDA software tools and laboratory equipment

CSD specific content

Chapter 1

Combinational Circuits

(50 h) – 2 ECTS

Chapter 2

Finite State Machines (FSM)

(50 h) – 2 ECTS

Chapter 3

Microcontrollers (μC)

(50h) – 2 ECTS

Laboratory skills: logic analysers, timing diagrams, debuggers/programmers, simulators, etc. …

- Proteus-VSM (virtual lab), WolframAlpha, Minilog, **VHDL** for developing and testing
- Quartus Prime (Intel), ispLEVER Classic – Diamond (Lattice Semiconductor), ISE – Vivado (AMD)
- Intel Integrated Synthesis, Synplify Pro synthesis (Synopsys), XST (Xilinx synthesis tools)
- ModelSim (Questa) Intel FPGA Edition (Siemens), Active HDL (Aldec) Lattice Edition, ISE simulator (Isim)

- Proteus-VSM (Labcenter Electronics)
- MPLABX (Microchip)
- XC8 compiler (Microchip)

MultiSim and Ultiboard

- Classic IC's
- sPLD GAL22V10

- Programmable logic devices (CPLD and FPGA) from Intel, Lattice, AMD.
- Training boards (DE10.Lite, DE2-115, Spartan 3AN Starter Kit, MachXO USB Starter Kit, NEXYS 2, etc.

- PIC 16F/18F, ATmega families of microcontrollers, Training boards PICDEM2+, etc.

CSD generic skills

English language	Oral and written communication	Self-directed learning	Teamwork	Project management

- Use English everywhere in CSD

- Pen & paper
- Thunderbird / Meet
- Video recordings

- Mindmaps, CMapTools,

- Cooperative learning

- Gantt charts

- Be systematic and try to write high quality reports asking for feedback
- Draw sketches, diagrams, concept maps, schematics and flowcharts
- Be active and participate. Be curious and **ask questions**
- Be constant, motivated and committed for the full semester

Planning activities and study time in and out of classroom (6 ECTS - 150 h)

Activities

- Theory and tutorial projects (P1 .. P12)
- Laboratory projects P_Ch1, P_Ch2 and P_Ch3 (including oral presentations)
- Individual questionnaires (Q1_4, Q5_8, Q9_12) and other classroom activities

Weekly study plan

Guided learning

- Classroom lectures (3 h)
  General discussion, theory, project tutorials and examples
- Laboratory project solving (2 h)
  Teamwork sessions, etc.

Self-directed learning

- **Student-conducted teamwork sessions**
- **Extra individual work**

(> 5 h)

15 weeks

10h per week

6 ECTS

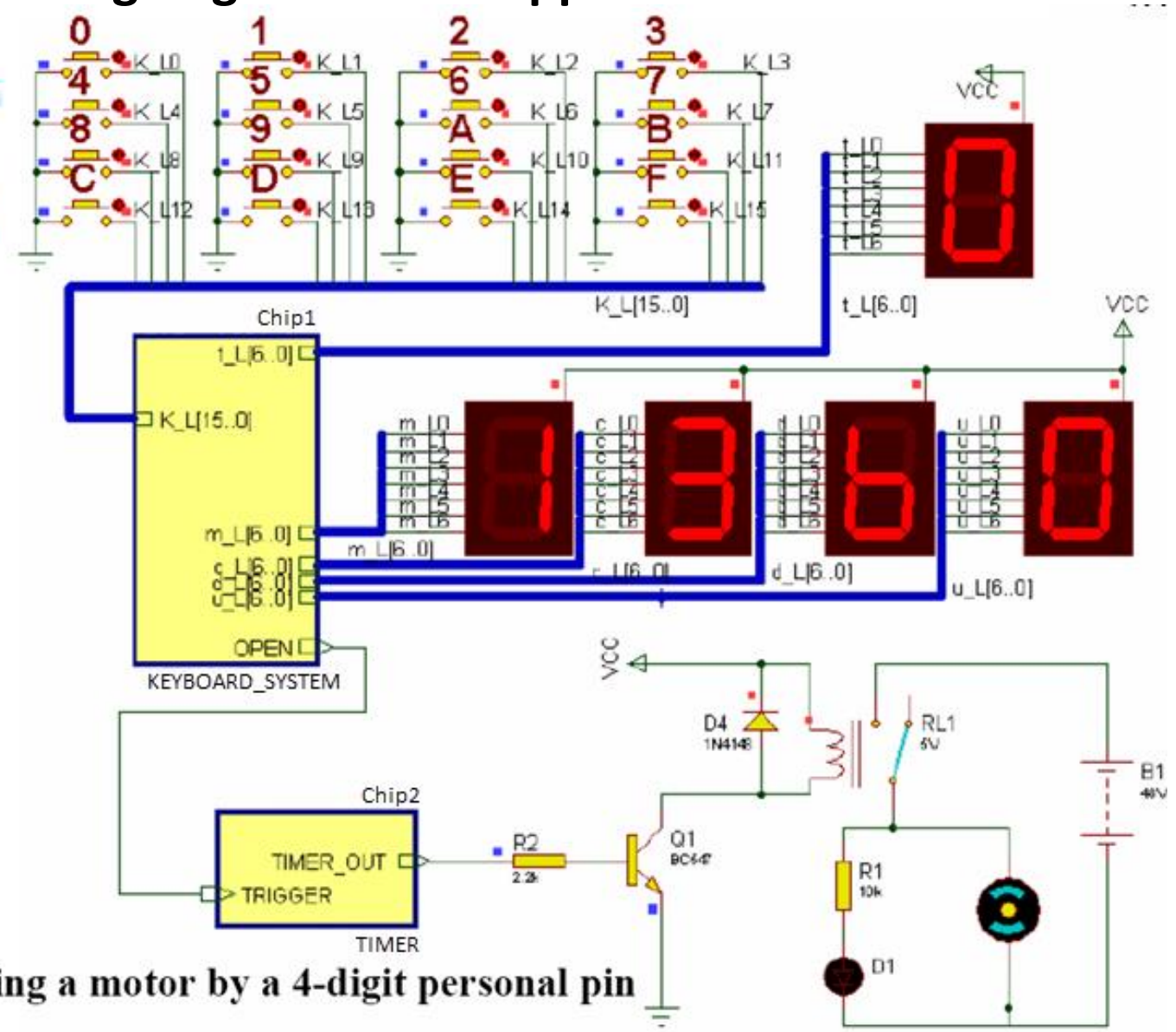
Activities/projects → Designing real-world applications

Real-world problems instead of pure academic exercises

→ **Motivation**

- using PLD/VHDL
- using microcontrollers/C

Comparison of alternative designs



Activating a motor by a 4-digit personal pin

Cooperative learning for designing projects

- **Positive interdependence**

  Team members are obliged to rely on one another to achieve their common goal

- **Individual accountability**

  All students in a group are held accountable for doing their share of the work and for mastery of all of the content to be learned

- **Face-to-face promotive interaction**

  Group members providing one another with feedback, challenging one another's conclusions and reasoning, and teaching and encouraging one another

- **Appropriate use of collaborative skills**

  Students are encouraged and helped to develop and practise skills in communication, leadership, decision-making, conflict management, and other aspects of effective teamwork

- **Regular self-assessment of group functioning**

  Team members periodically assess what they are doing well as a team and what they need to work on for functioning more effectively in the future

Web pages as an ebook and agenda

Digital Circuits and Systems (CSD - *digsys*)

Learning outcomes, organisation and projects

Chapter 1	Chapter 2	Chapter 3
Combinational circuits	**Sequential systems**	**Microcontrollers**

P12: Peripherals: timers, A/D, etc.

P11: Peripherals: LCD display.

P10: Implementing FSM in C language. Interrupts.

P9: Microcontroller architecture. Digital I/O.

digsys.upc.edu

P8: Dedicated processors: datapath, control unit and CLK generators.

P7: Standard sequential systems: counters, data and shift registers.

P6: Finite state machines (FSM): synchronous canonical sequential systems.

P5: 1-bit memory cells. Analysis of circuits based on latches and flip-flops.

P4: Standard arithmetic circuits (2C, integers) and ALU. Propagation time and computing speed.

P3: Standard arithmetic circuits (radix-2): adders, comparators, etc. Structural/hierarchical VHDL (plan C2).

P2: Standard logic circuits: *mux*, *demux*, *dec*, *enc*, etc. Flat VHDL: logic equations (plan A), behavioural (plan B).

P1: Logic gates and Boolean algebra. Analysis and design: schematics, truth table, minterms, maxterms, SoP, PoS.

Cross-curricular skills Atenea

Chapter 1: Combinational circuits

W1	L1.1		L1.2			L1.3	L1.4			L1.5									
W2			L1.6	L2.1				LAB1.1			L2.2				PLA1.1				
W3				L2.3	L2.4				LAB1.2			L2.5			PLA1.1	PLA1.2			
W4					L3.1	L3.2					LAB2		L3.3			PLA1.2	PLA2		
W5						L4.1	L4.2					LAB3		L4.3			PLA2	PLA3	
W6													LAB4		AR1			PLA3	PLA4	Q1-4

Midterm exam

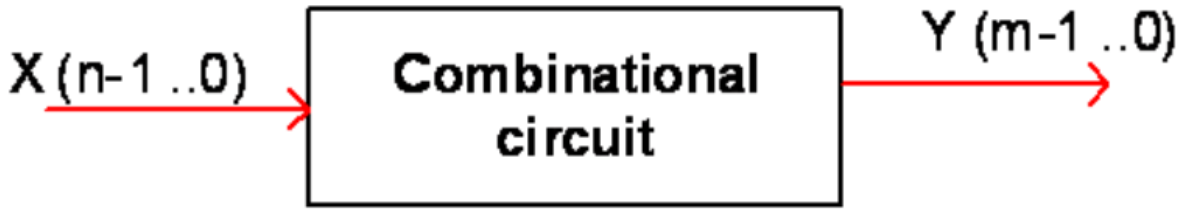


Fig. 1. Symbol of a generalised combinational circuit. This block is described by its truth table or the equivalent canonical equations product of maxterms or sum of minterms.

P_Ch1 post laboratory assigments after having practised in lectures and lab sessions:

PLA1.1	Due date February 28	Circuit analysis using Proteus (method II) and Wolfram Alpha (method IV)
PLA1.2	March 6	Circuit analysis using VHDL tools (method III)
PLA2	March 13	Circuit design using single-VHDL file plan A and plan B
PLA3	March 24	Circuit design using multiple-file hierarchical plan C2
PLA4	April 10	Gate level measurements: how fast is a circuit operating?

Q & A

Planning session by session

Example projects and support

- Exams and discussion from previous semesters
- Collection of sample and tutorial problems and projects
- Example questionnaires
- Threads of comments and queries related to tutorial and post-lab projects
- Combined with (asynchronous) email support (rules) and (synchronous) meet

BIBLIOGRAPHY → digsys.upc.edu/csd/books/books.html

Assessment scheme

- Exams = 50%
- Questionnaires and class activities 20%
- Projects (P_Ch) = 30%

Provisional grading available at Atenea.

Project organisation (at least four sheets of paper):

1)Specifications
2)Planning
3)Development
4)Test and verification
5)Report (handwritten)
6)Prototyping and laboratory measurements

Course policies

NOTE: To get marks → project solutions have to be submitted in the established format and before the due date.

Exams will be sit at school premises. Only pen, paper and scientific calculator.

Class attendance is requested (even if it is not an obligation). You must engage participating actively in class and promoting cooperation in your lab group.

Laboratory attendance is compulsory.

Academic dishonesty. Cheating penalties:

- First instance → 0 on corresponding assignment
- Second → 0 for entire course

Grades will NOT change because you really worked hard on class, or you need to graduate, or because otherwise you will lose your grant.

Do you want a good grade? Earn it with your full commitment and designing high quality projects.