CSD: Designing circuits in VHDL (Concept map)

Symbol

Examples of commercial chips

Truth table, equations, algorithm or other high-level description

Combinational circuit
(standard logic, arithmetic or any kind of circuit)

How to expand it?

Related to **Plan C2**

Special inputs and outputs: enable, ripple, etc.

Timing diagram

How to design it?
(using VHDL tools)

Related to **VHDL SIMULATION**

Circuit_tb.vhd

Related to **VHDL SYNTHESIS**

Circuit.vhd

Plan **A**

Structural description

Any kind of equation

Minimised equations (minilog)

Canonical equations

Flat design: a single VHDL file

Plan **B**

Behavioural description
(truth table, algorithms, etc.)

Plan **C1**

Building blocks

Hierarchical. (Not practical: logic, blocks, equations in a single file)

Plan **C2**

Building blocks

Hierarchical design using COMPONENTS & SIGNALS
Recommended for **large circuits**

Multiple VHDL file design

Other strategies
(not in CSD)

Any other plan is possible when you've got some experience. Engineer's creativity and imagination. (Advanced or master courses, research)