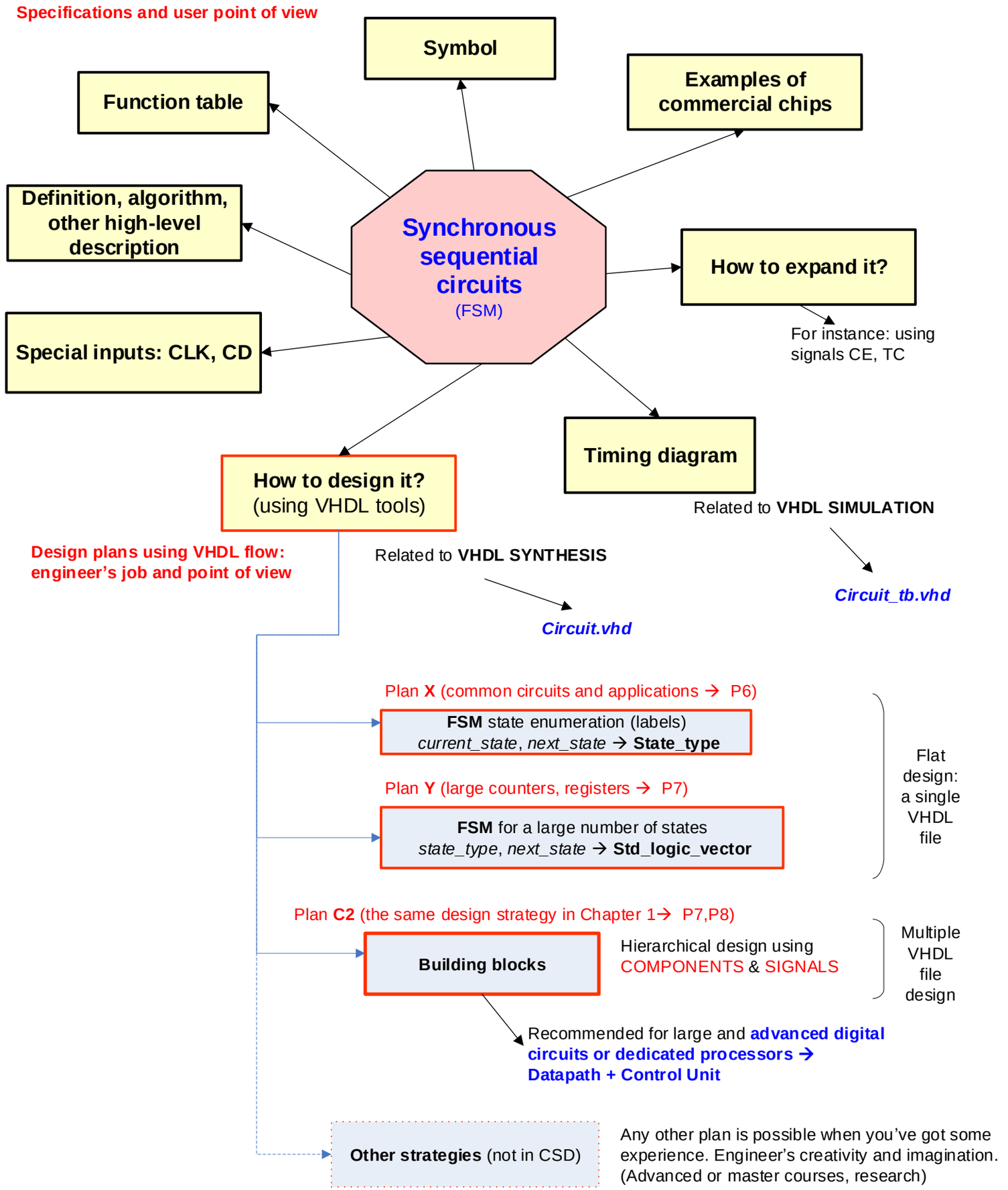
CSD – Chapter 2.
Designing synchronous sequential circuits in VHDL (Concept map)



Design plans (continuation) →

Remember that each plan becomes an EDA project producing different circuit synthesis (RTL) and technology schematics
→ CPLD, FPGA chips resources used (logic elements, registers, etc.

How to design it?
(using VHDL tools)

Plan **X** (common circuits and applications → P6)

FSM state enumeration (labels)
state_type, *next_state* → state_type

Plan **Y** (large counters, registers → P7)

FSM for a large number of states
state_type, *next_state* → STD_LOGIC_VECTOR

- State encoding and number of *D_FF* registers.
- Draw the state register based on *D_FF*.
- CC2 truth table and flowchart (behavioural interpretation of the combinational circuit)
- CC1 truth table and flowchart (behavioural interpretation of the combinational circuit)

Plan **C2** (as in Chapter 1 (P3, P4) → P7, P8)

Building blocks

- How to invent an schematic composed of multiple components, signals and logic?
- How many VHDL files the project will include?
- What is the project location?

Development using hardware EDA tools for transforming our ideas (by means of VHDL files) into real-world and usable circuits