WHITE PAPER

High-Speed Digital Design Success Demands A Modern Workflow

KEYSIGHT

PATHWAVE

Multifunction, always-on connected devices and systems dominate today's high-speed digital (HSD) design trends. New smart or IoT (Internet of Things) devices feature increasing levels of complexity and lower consumption of power in smaller rugged packages. For example, smart cars combine sensors with a powerful onboard computer and complex communication systems that connect to the internet, GPS, other cars, and traffic lights (Figure 1).

In addition to complexity, power, and space constraints, the race continues for faster data transmission. The most common consumer products already provide gigabit data speeds. Cloud data is driving the need for server farms with 400 Gb Ethernet communications and ever-higher bandwidth.

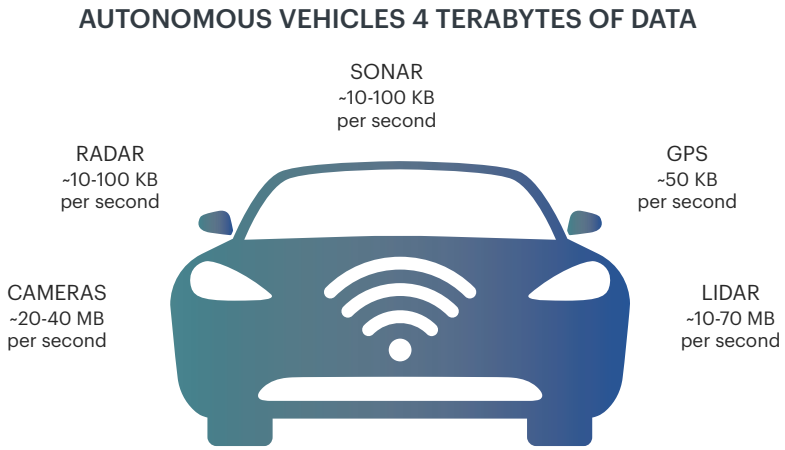


Figure 1. Autonomous vehicles generate huge amounts of data from HSD subsystems

Exponential growth of design and test requirements is one consequence of increasing electronic complexity. Take, for example, 5G wireless, which requires 20x the number of conformance tests as its LTE predecessor. Add technologies such as Wi-Fi, *Bluetooth*®, multiple radios, digital memory, and high-speed input/output into the mix, and the resulting mountains of data clearly strain current capabilities to manage design and test configurations. Further complicating the matter are local standards that electronic designers must pass in more than 20 world geographies.

A simulation and measurement-based workflow enables Power Integrity engineers to design resonant-free power delivery and avoid rogue voltage waves.

Predicting Electromagnetic Interference and Compliance Is Paramount

Failing a compliance test (e.g., conducted emissions) at the end of the product design cycle is expensive. Old electromagnetic interference reduction approaches based on adding components or re-spinning designs are costly and time-consuming. Retrofits with added filters and capacitors increase manufacturing costs, while design re-spins to fix electromagnetic interference / compliance (EMI / EMC) problems result in product delays and lost revenue.

It is more effective to start early in the design phase to understand and mitigate potential EMI noise sources. Power delivery is the one network that connects to everything in a design, providing a path for conducted EMI noise to propagate through a system. The fast-changing di / dt transients of the switching converters or load demand can easily interact with parasitic inductances to cause excessive Ldi/dt power rail noise.

This specialized power delivery for HSD has evolved into the field of power integrity (PI) engineering. Modern design tool suites and methodology enable PI engineers to simulate potential EMI sources and predict compliance up front. Whether parasitic effects impact a design depends on the desired compliance specification, the performance margin built into the design, and the manufacturing and process tolerances.

Data Sheets Do Not Reveal Worst-Case Voltage Noise Ripple for Fast PDNs

In a world of increasing power distribution network (PDN) complexity, as in autonomous vehicles, power delivery is no longer a DC problem. HSD data requires fast delivery of power at microwave frequencies. An autonomous vehicle PDN serves data collected from cameras, radar, sonar, GPS, and lidar subsystems that can easily reach 4 TB per day (Figures 1 and 2). The vehicle processes data locally and requires processors, DDR memory, serializer / deserializer Tx / Rx devices, each with its own point-of-load (POL) power supply. Fast di / dt switching loads from these subsystems can react with any inductance in the power delivery path to create voltage noise ripple. The amount of allowable ripple continues to decrease as power rail voltages drop below 1 V to meet low power demands and faster data rates.

Note: A POL power supply is typically a switched mode power supply with a buck regulator DC-DC converter design. The microprocessor printed circuit board world calls this a voltage regulator module. All these terms are interchangeable and refer to the source of power.

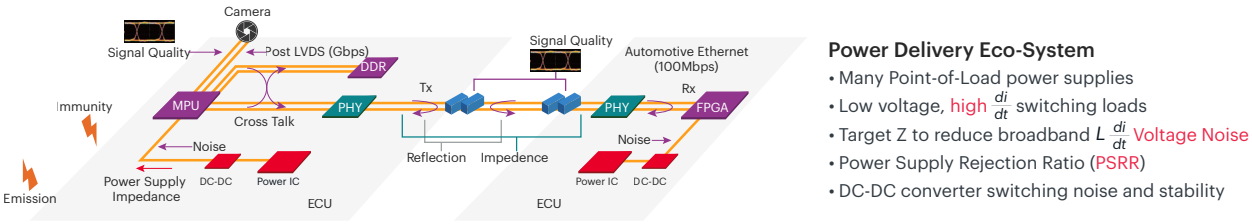


Figure 2. In this autonomous vehicle PDN exemplary of today's complex power delivery ecosystem, power integrity is about fast delivery of power at microwave frequencies

PDNs must provide clean power to the load. Electronic devices have maximum voltages and ripple specifications to avoid damage, lost data, and EMI / EMC failures. The goal of the power rail is to provide a constant voltage even when the current load is switched on and off with high-frequency di / dt transients. Traditional methods of measuring noise on a power rail often fail to detect worst-case voltage ripple.

To test the power rail, PI engineers typically use the classic step load excitation taken from most data sheets. When a step load change in current is applied to the voltage rail, engineers refer to the corresponding response on the power rail as the natural response. The natural response will often have some ringing, but it decays exponentially. The small-voltage ripple the step load generates could easily pass specifications.

When the load excites the power rail at that ripple frequency, it is known as forced response (Figure 3). The forced response of a resonance is much larger and represents the worst-case ripple on the power rail. The forced response grows exponentially to a steady-state value. It can be large enough to cause a device damaging over voltage, a failure in data transmission, and EMI noise. Normal operation of the load may never excite this resonant frequency, but digital systems are wideband and difficult to test for all combinations of operating scenarios. For example, power-saving modes that turn on and off and data bursts can easily create HSD load transients that extend from kilohertz to gigahertz.

Individual data sheets for electronic components do not contain enough information about the end user application to provide worst-case forced response data. The distributed inductance of the printed circuit board (PCB), interconnects, and decoupling capacitors creates a complex dynamic behavior that is not obvious in the over-simplified step response. Modern simulation tools that handle electromagnetic simulation of the PCB wiring enable PI engineers to analyze this complexity to identify and mitigate problems early in the design process.

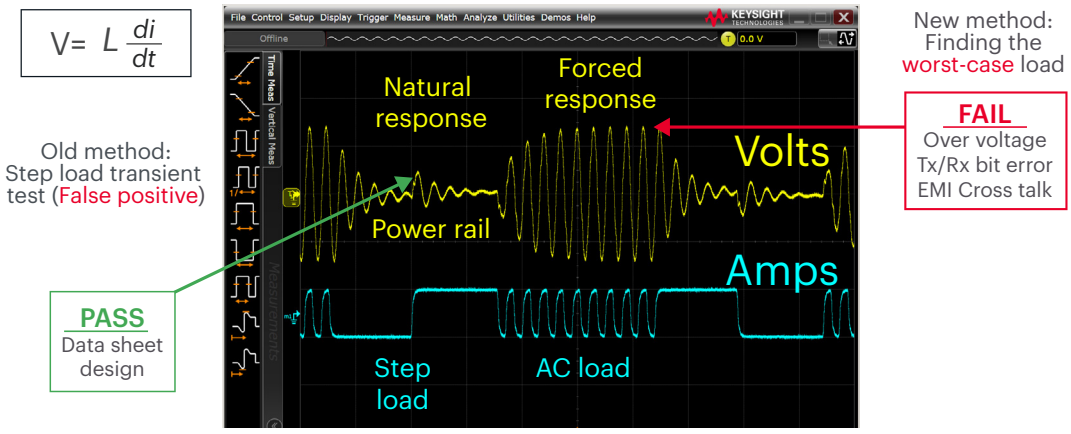


Figure 3. In this power rail measurement made on a real-time oscilloscope, the yellow trace shows the power rail voltage amplitude vs. time, while the blue trace shows the corresponding load current amplitude vs. time

Key takeaway:

Forced response is worst-case, not the data sheet step load

The modern workflow method of testing for the worst-case voltage ripple is to look at the impedance peaks in the frequency domain (Figure 4). PI engineers must identify the power rail impedance peaks where the di / dt at those frequencies, multiplied by the impedance, results in a maximum ripple. If the peaks are below a target impedance (flat green dashed line), the voltage ripple at that peak frequency will be within acceptable limits.

However, what happens if the second impedance peak frequency is excited at the maximum of the forced response of the first frequency, and the third impedance peak frequency is excited at the maximum of the first two? Just like two ocean waves lining up to create one large rogue wave, multiple resonances can line up to create a rogue voltage wave on the power rail. Although their probability is low, rogue voltage waves do exist. Passengers in next-generation autonomous vehicles should not have to take a chance on rogue waves. Especially when modern simulation and measurement workflows can go beyond the data sheet to mitigate problems early in the design process.

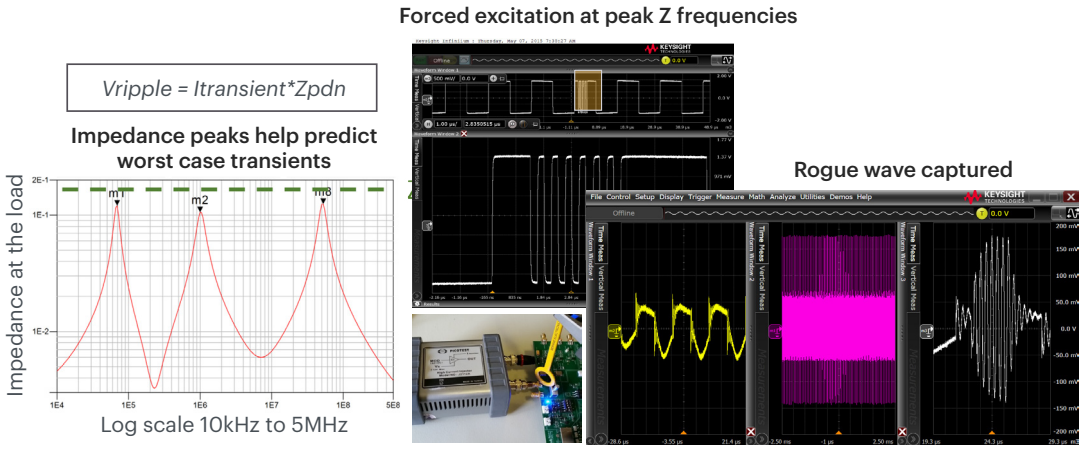


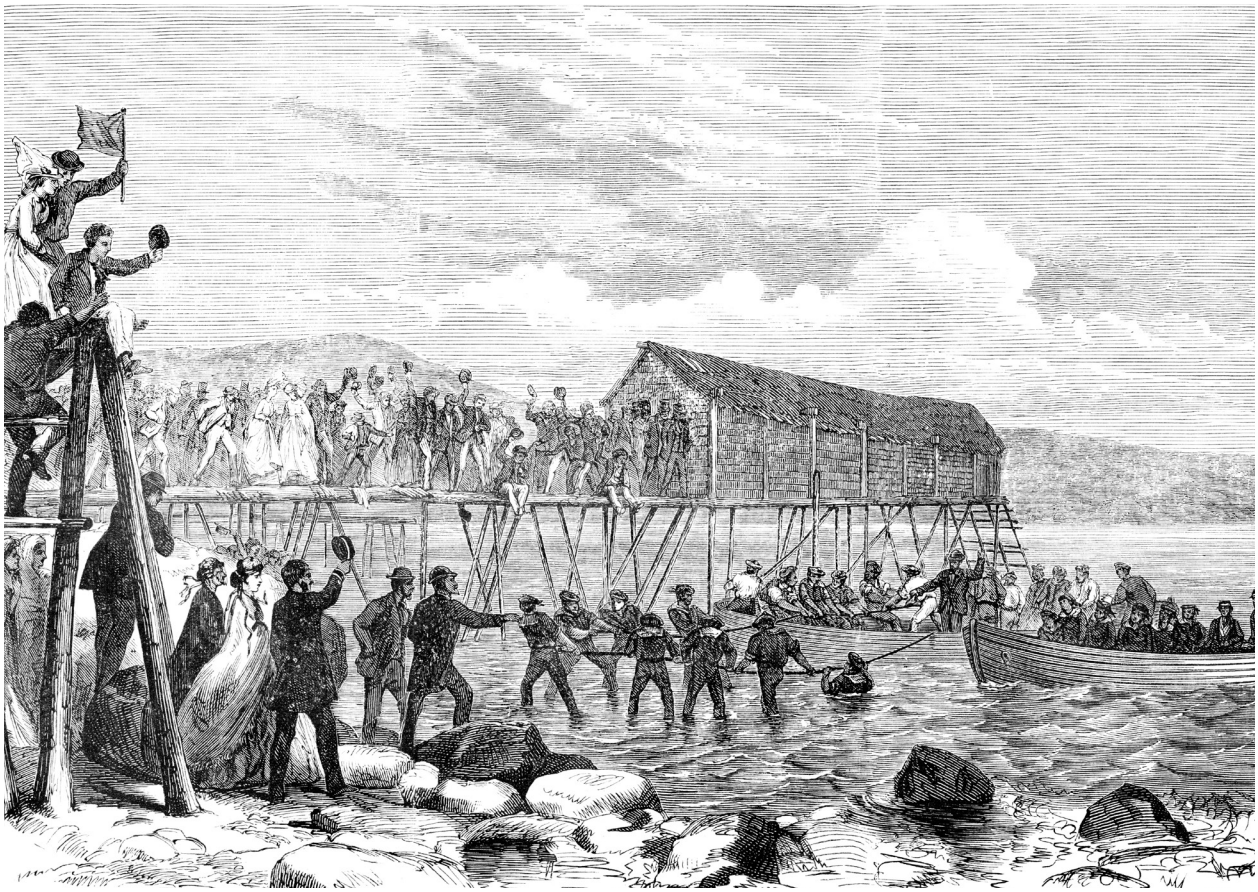
Figure 4. Multiple impedance peaks in the frequency domain result in power rail ripple and can be a source of rogue voltage waves

Key takeaway:

Voltage rogue waves are real

Epic Failure: The Transatlantic Telegraph Cable

The original design of the transatlantic cable, shown here arriving at Heart's Content, Newfoundland, looked simple. What could be so difficult about stretching a wire between a transmitter and a receiver? After the huge expense and time spent installing the cable across the Atlantic Ocean, the first test in 1858 found such poor signal quality that operators had to slow transmission to an almost unusable speed. The following month, electrician Wildman Whitehouse destroyed the cable by applying excessive voltage to it while trying to achieve faster operation. Where were the signal and power integrity engineers to explain AC impedance?



In summary, PI engineers can no longer afford to wait until after layout to perform measurements that find EMI on the PDN. The cost associated with failing EMC late in the design cycle is too high. Starting at post-layout electromagnetic analysis often leads to optimization of a bad design causing re-spins. Starting with pre-layout to explore the right design space before going to layout and optimization saves both re-spin expense and cycle time.

Using simulation tools as part of a modern PI workflow prevents failures late in the HSD design process. Moving from a traditional data sheet-based approach to a modern simulation and measurement-based workflow produces higher quality HSD designs with resonant free PDNs that avoid rogue voltage waves.

For more information on how to succeed in HSD design using a modern workflow, go to PathWave Platform.

Additional Resources:

- Application Note: *Optimize Power Distribution Networks for Flat Impedance* 5992-4272EN