

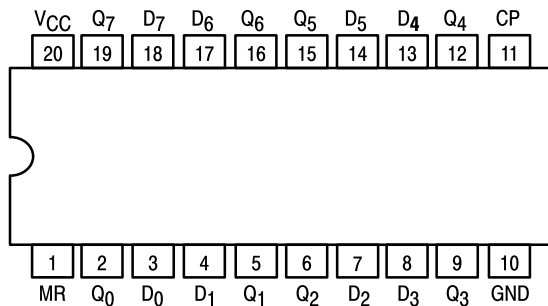


# OCTAL D FLIP-FLOP WITH CLEAR

The SN54/74LS273 is a high-speed 8-Bit Register. The register consists of eight D-Type Flip-Flops with a Common Clock and an asynchronous active LOW Master Reset. This device is supplied in a 20-pin package featuring 0.3 inch lead spacing.

- 8-Bit High Speed Register
- Parallel Register
- Common Clock and Master Reset
- Input Clamp Diodes Limit High-Speed Termination Effects

## CONNECTION DIAGRAM DIP (TOP VIEW)



### PIN NAMES

CP Clock (Active HIGH Going Edge) Input  
 D<sub>0</sub>-D<sub>7</sub> Data Inputs  
 MR Master Reset (Active LOW) Input  
 Q<sub>0</sub>-Q<sub>7</sub> Register Outputs (Note b)

### LOADING (Note a)

	HIGH	LOW
CP	0.5 U.L.	0.25 U.L.
D <sub>0</sub> -D <sub>7</sub>	0.5 U.L.	0.25 U.L.
MR	0.5 U.L.	0.25 U.L.
Q <sub>0</sub> -Q <sub>7</sub>	10 U.L.	5 (2.5) U.L.

### NOTES:

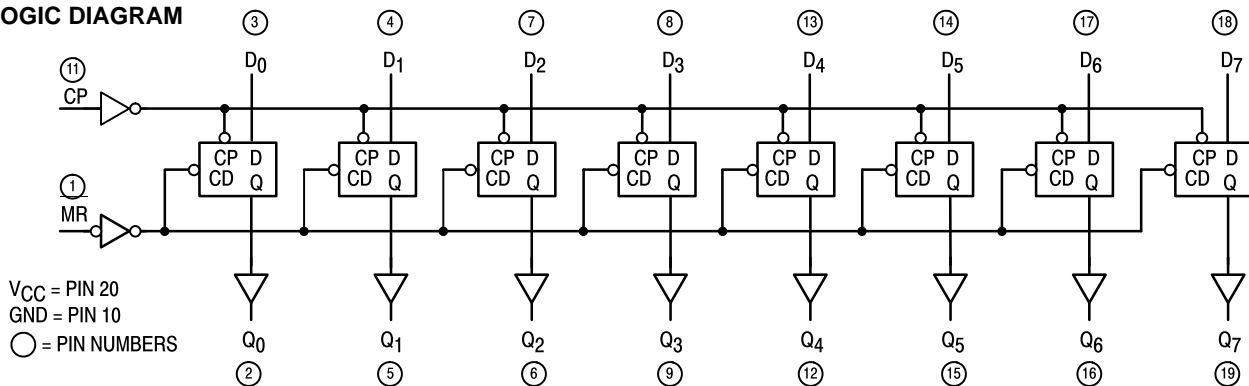
- a) 1 TTL Unit Load (U.L.) = 40  $\mu$ A HIGH/1.6 mA LOW.  
 b) The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

### TRUTH TABLE

MR	CP	D <sub>x</sub>	Q <sub>x</sub>
L	X	X	L
H		H	H
H		L	L

H = HIGH Logic Level  
 L = LOW Logic Level  
 X = Immaterial

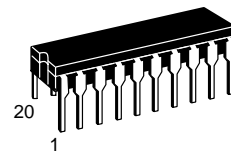
### LOGIC DIAGRAM



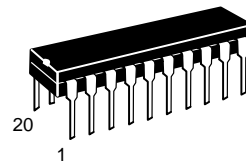
V<sub>CC</sub> = PIN 20  
 GND = PIN 10  
 ○ = PIN NUMBERS

## SN54/74LS273

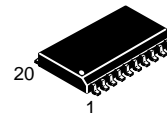
OCTAL D FLIP-FLOP WITH CLEAR  
 LOW POWER SCHOTTKY



J SUFFIX  
 CERAMIC  
 CASE 732-03



N SUFFIX  
 PLASTIC  
 CASE 738-03



DW SUFFIX  
 SOIC  
 CASE 751D-03

### ORDERING INFORMATION

SN54LSXXXJ Ceramic  
 SN74LSXXXN Plastic  
 SN74LSXXXDW SOIC

# SN54/74LS273

## FUNCTIONAL DESCRIPTION

The SN54/74LS273 is an 8-Bit Parallel Register with a common Clock and common Master Reset.

When the MR input is LOW, the Q outputs are LOW,

independent of the other inputs. Information meeting the setup and hold time requirements of the D inputs is transferred to the Q outputs on the LOW-to-HIGH transition of the clock input.

## GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V <sub>CC</sub>	Supply Voltage	54	4.5	5.0	5.5	V
		74	4.75	5.0	5.25	
T <sub>A</sub>	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I <sub>OH</sub>	Output Current — High	54, 74			-0.4	mA
I <sub>OL</sub>	Output Current — Low	54			4.0	mA
		74			8.0	

## DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits			Unit	Test Conditions
			Min	Typ	Max		
V <sub>IH</sub>	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V <sub>IL</sub>	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V <sub>IK</sub>	Input Clamp Diode Voltage			-0.65	-1.5	V	V <sub>CC</sub> = MIN, I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	54	2.5	3.5		V	V <sub>CC</sub> = MIN, I <sub>OH</sub> = MAX, V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> per Truth Table
		74	2.7	3.5		V	
V <sub>OL</sub>	Output LOW Voltage	54, 74		0.25	0.4	V	V <sub>CC</sub> = V <sub>CC</sub> MIN, V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> per Truth Table
		74		0.35	0.5	V	
I <sub>IH</sub>	Input HIGH Current				20	μA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 2.7 V
					0.1	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 7.0 V
I <sub>IL</sub>	Input LOW Current				-0.4	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 0.4 V
I <sub>OS</sub>	Short Circuit Current (Note 1)		-20		-100	mA	V <sub>CC</sub> = MAX
I <sub>CC</sub>	Power Supply Current				27	mA	V <sub>CC</sub> = MAX

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

## AC CHARACTERISTICS (T<sub>A</sub> = 25°C, V<sub>CC</sub> = 5.0 V)

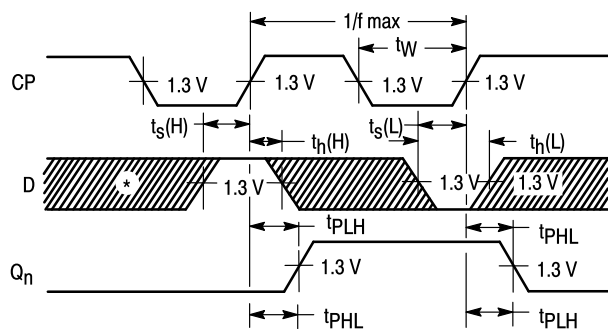
Symbol	Parameter		Limits			Unit	Test Conditions
			Min	Typ	Max		
f <sub>MAX</sub>	Maximum Input Clock Frequency		30	40		MHz	Figure 1
t <sub>PHL</sub>	Propagation Delay, MR to Q Output			18	27	ns	Figure 2
t <sub>PLH</sub>	Propagation Delay, Clock to Output			17	27	ns	Figure 1
t <sub>PHL</sub>				18	27		

# SN54/74LS273

## AC SETUP REQUIREMENTS ( $T_A = 25^\circ\text{C}$ , $V_{CC} = 5.0\text{ V}$ )

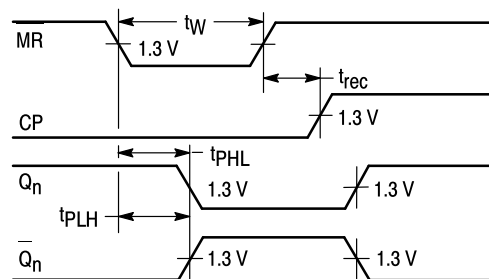
Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
$t_w$	Pulse Width, Clock or Clear	20			ns	Figure 1
$t_s$	Data Setup Time	20			ns	Figure 1
$t_h$	Hold Time	5.0			ns	Figure 1
$t_{rec}$	Recovery Time	25			ns	Figure 2

## AC WAVEFORMS



\*The shaded areas indicate when the input is permitted to change for predictable output performance.

**Figure 1. Clock to Output Delays, Clock Pulse Width, Frequency, Setup and Hold Times Data to Clock**



**Figure 2. Master Reset to Output Delay, Master Reset Pulse Width, and Master Reset Recovery Time**

## DEFINITION OF TERMS

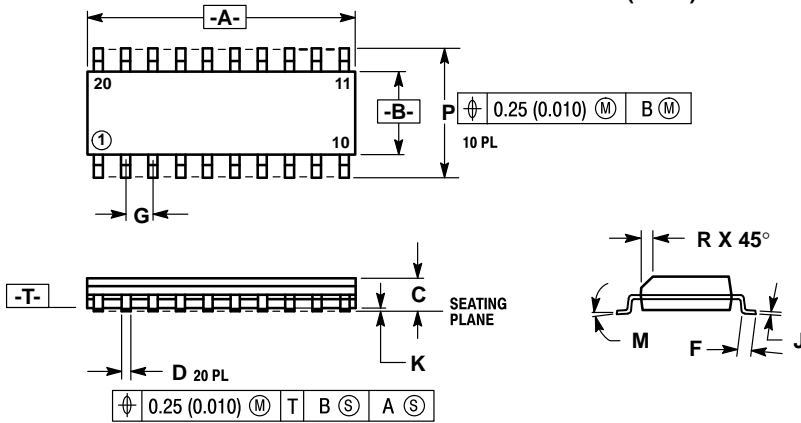
**SETUP TIME ( $t_s$ )** — is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW-to-HIGH in order to be recognized and transferred to the outputs.

**HOLD TIME ( $t_h$ )** — is defined as the minimum time following the clock transition from LOW-to-HIGH that the logic level must be maintained at the input in order to ensure continued

recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW-to-HIGH and still be recognized.

**RECOVERY TIME ( $t_{rec}$ )** — is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW-to-HIGH in order to recognize and transfer HIGH data to the Q outputs.

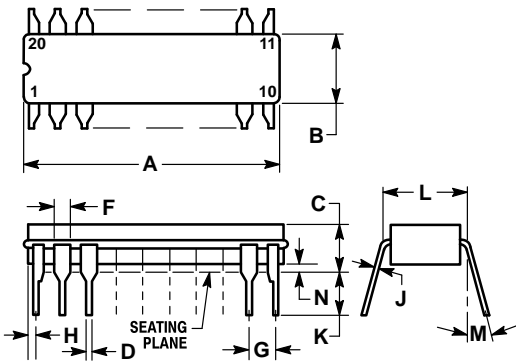
**Case 751D-03 DW Suffix  
20-Pin Plastic  
SO-20 (WIDE)**



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
  4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
  5. 751D-01, AND -02 OBSOLETE, NEW STANDARD 751D-03.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	12.65	12.95	0.499	0.510
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC	0.050 BSC		
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

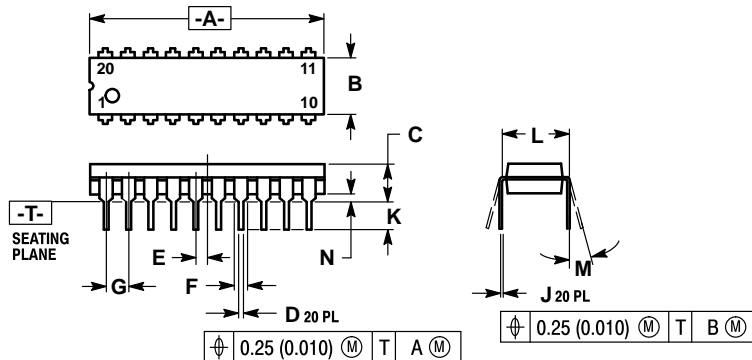
**Case 732-03 J Suffix  
20-Pin Ceramic Dual In-Line**



- NOTES:
1. LEADS WITHIN 0.25 mm (0.010) DIA., TRUE POSITION AT SEATING PLANE, AT MAXIMUM MATERIAL CONDITION.
  2. DIM L TO CENTER OF LEADS WHEN FORMED PARALLEL.
  3. DIM A AND B INCLUDES MENISCUS.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	23.88	25.15	0.940	0.990
B	6.60	7.49	0.260	0.295
C	3.81	5.08	0.150	0.200
D	0.38	0.56	0.015	0.022
F	1.40	1.65	0.055	0.065
G	2.54 BSC	0.100 BSC		
H	0.51	1.27	0.020	0.050
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	7.62 BSC	0.300 BSC		
M	0°	15°	0°	15°
N	0.25	1.02	0.010	0.040

**Case 738-03 N Suffix  
20-Pin Plastic**



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.
  3. DIMENSION "L" TO CENTER OF LEAD WHEN FORMED PARALLEL.
  4. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
  5. 738-02 OBSOLETE, NEW STANDARD 738-03.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	25.66	27.17	1.010	1.070
B	6.10	6.60	0.240	0.260
C	3.81	4.57	0.150	0.180
D	0.39	0.55	0.015	0.022
E	1.27 BSC	0.050 BSC		
F	1.27	1.77	0.050	0.070
G	2.54 BSC	0.100 BSC		
J	0.21	0.38	0.008	0.015
K	2.80	3.55	0.110	0.140
L	7.62 BSC	0.300 BSC		
M	0°	15°	0°	15°
N	0.51	1.01	0.020	0.040

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SYMBOL	SW1	SW2
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tpZL	Closed	Open
tpLZ	Closed	Closed

