DATA SHEET

74LVC169
Presettable synchronous 4-bit up/down binary counter

specification
Supersedes data of 1996 Aug 23
IC24 Data Handbook

1998 May 20

Philips Semiconductors

PHILIPS

Presettable synchronous 4-bit up/down binary counter

74LVC169

FEATURES

- Wide supply voltage range of 1.2 V to 3.6 V
- In accordance with JEDEC standard no. 8-1A
- Inputs accept voltages up to 5.5 V
- CMOS low power consumption
- Direct interface with TTL levels
- Synchronous counting and loading
- Up/down counting
- Modular 16 binary counter
- Two count enable inputs for n-bit cascading
- Built-in lookahead carry capability
- Presettable for programmable operation
- Positive-edge triggered clock

DESCRIPTION

The 74LVC169 is a high-performance, low-power, low-voltage, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

The 74LVC169 is a synchronous presettable binary counter which features an internal lookahead carry and can be used for high-speed counting. Synchronous operation is provided by having all flip-flops clocked simultaneously on the positive-going edge of the clock (CP). The outputs (Q_0 to Q_3) of the counters may be preset to a HIGH or LOW level. A LOW level at the parallel enable input (PE) disables the counting action and causes the data at the data inputs (D_0 to D_3) to be loaded into the counter on the positive-going edge of the clock (provided that the set-up and hold time requirements for PE are met). Preset takes place regardless of the levels at count enable inputs (CEP and CET). A low level at the master reset input (MR) sets all four outputs of the flip-flops (Q_0 to Q_3) to LOW level after the next positive-going transition on the clock (CP) input (provided that the set-up and hold time requirements for PE are met).

This action occurs regardless of the levels at CP, $\overline{\text{PE}}$, CET and CEP inputs This synchronous reset feature enables the designer to modify the maximum count with only one external NAND gate.

The lookahead carry simplifies serial cascading of the counters. Both count enable inputs (CEP and CET) must be HIGH to count. The CET input is fed forward to enable the terminal count output (TC). The TC output thus enabled will produce a HIGH output pulse of a duration approximately equal to a HIGH level output of Q_0. This pulse can be used to enable the next cascaded stage. The maximum clock frequency for the cascaded counters is determined by the CP to TC propagation delay and CEP to CP set-up time, according to the following formula:

$$f_{max} = \frac{1}{tp_{(max)}\text{ (CP to TC)} + t_{SU}\text{ (CEP to CP)}}$$

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $T_R = T_F \leq$ 2.5ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay CP to Q_n CP to $\overline{\text{TC}}$ $\overline{\text{CET}}$ to $\overline{\text{TC}}$	C_L = 50 pF V_{CC} = 3.3V	 5.0 6.5 5.3	ns
f_{MAX}	maximum clock frequency		200	MHz
C_I	input capacitance		5.0	pF
C_{PD}	power dissipation capacitance per gate	notes 1 and 2	42	pF

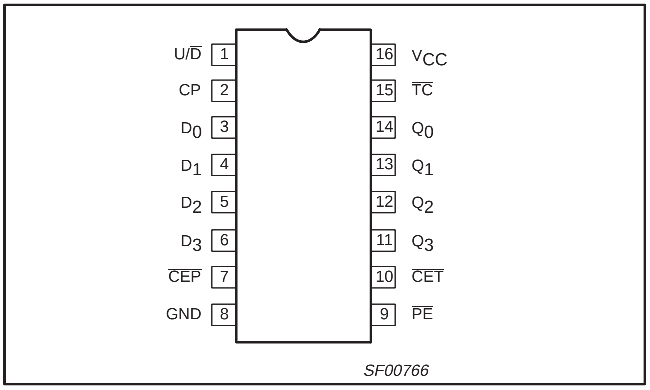
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs
2. The condition is V_1 = GND to V_{CC}

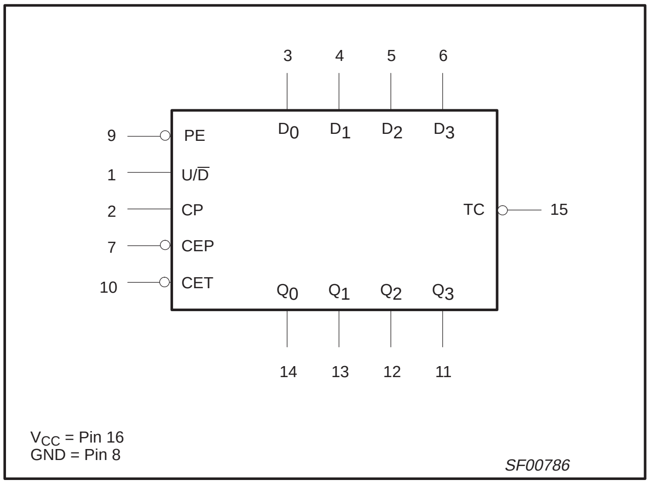
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
16-Pin Plastic SO	–40°C to +85°C	74LVC169 D	74LVC169 D	SOT109-1
16-Pin Plastic SSOP Type II	–40°C to +85°C	74LVC169 DB	74LVC169 DB	SOT338-1
16-Pin Plastic TSSOP Type I	–40°C to +85°C	74LVC169 PW	74LVC169PW DH	SOT403-1

PIN CONFIGURATION



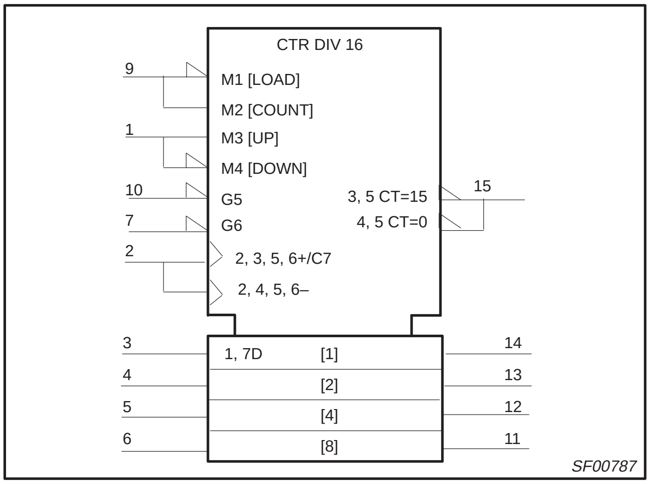
LOGIC SYMBOL



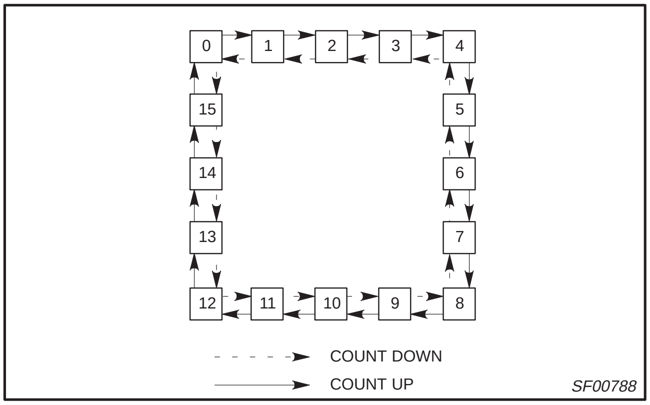
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	U/$\overline{D}$	up/down control input
2	CP	clock input (LOW-to-HIGH, edge-triggered)
3,4,5,6	D_0 to D_3	data inputs
7	CEP	count enable inputs (active LOW)
8	GND	ground (0V)
9	$\overline{PE}$	parallel enable input (active LOW)
10	CET	count enable carry input (active LOW)
14,13,12,11	Q_0 to Q_3	flip-flop outputs
15	TC	terminal count output (active LOW)
16	V_{CC}	positive supply voltage

LOGIC SYMBOL (IEEE/IEC)



STATE DIAGRAM

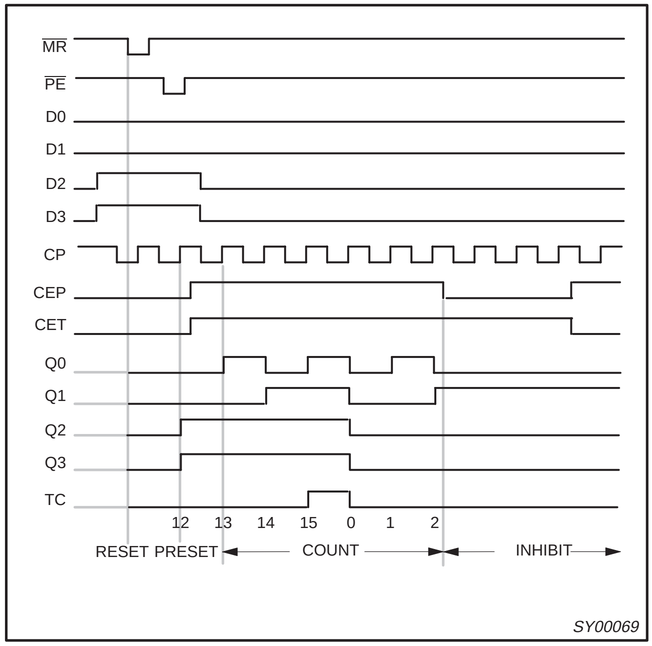


FUNCTION TABLE

OPERATING MODES	INPUTS						OUTPUTS	
	CP	U/$\overline{D}$	$\overline{CEP}$	$\overline{CET}$	$\overline{PE}$	D_n	Q_n	$\overline{TC}$
Parallel load (Dn→Qn)	↑	X	X	X	l	l	L	*
	↑	X	X	X	X	X	H	*
Count Up (increment)	↑	h	l	l	h	X	Count Up	*
Count Down (decrement)	↑	l	l	l	h	X	Count Down	*
Hold (do nothing)	↑	X	h	X	h	X	q_n	*
	↑	X	X	X	h	X	q_n	H

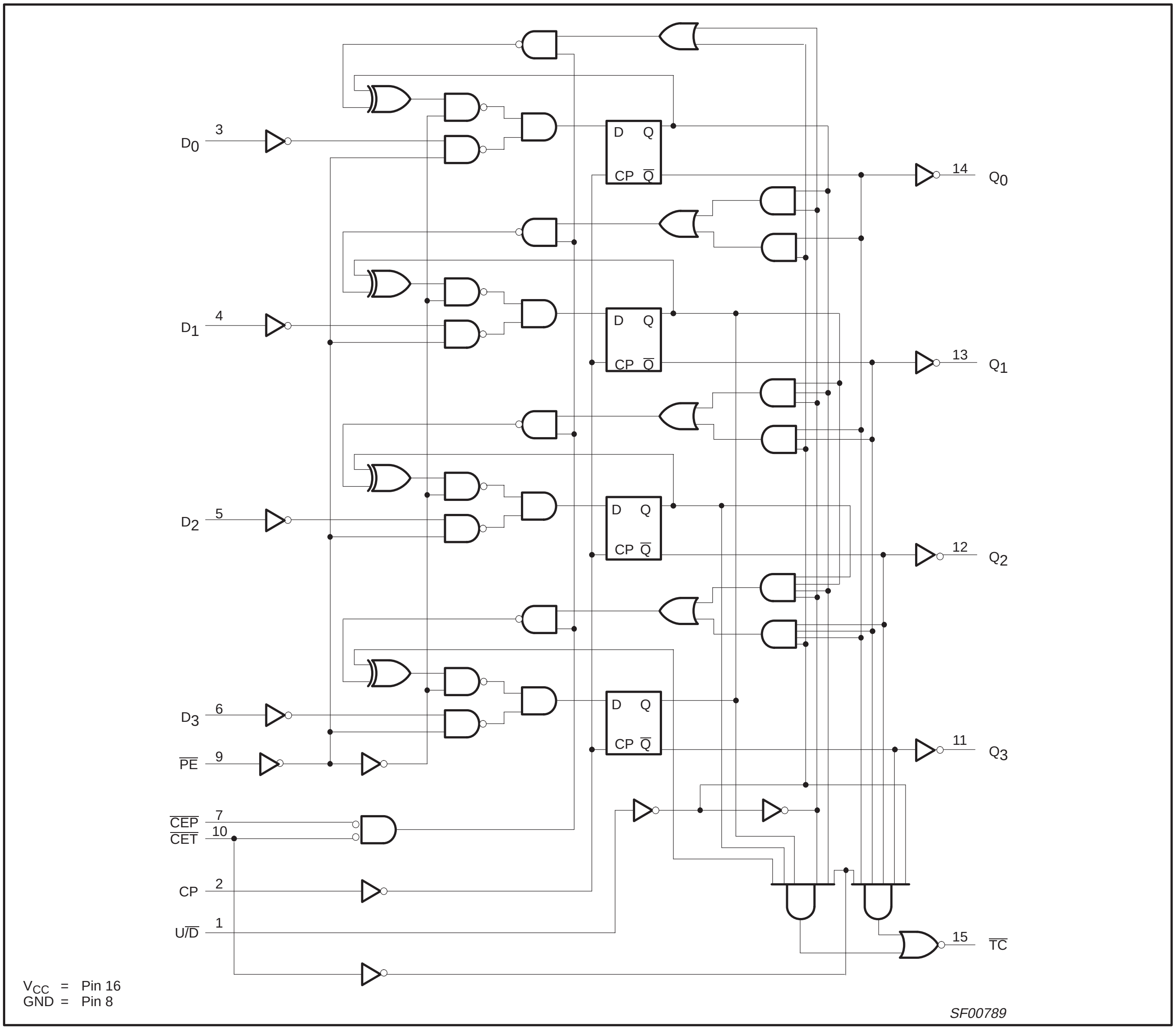
H = High voltage level steady state
h = High voltage level one setup time prior to the Low-to-High clock transition
L = Low voltage level steady state
l = Low voltage level one setup time prior to the Low-to-High clock transition
q = Lower case letters indicate the state of the referenced output prior to the Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition
* = The $\overline{TC}$ is Low when $\overline{CET}$ is Low and the counter is at Terminal Count.
Terminal Count Up is (HHHH) and Terminal Count Down is (LLLL).

TYPICAL TIMING SEQUENCE

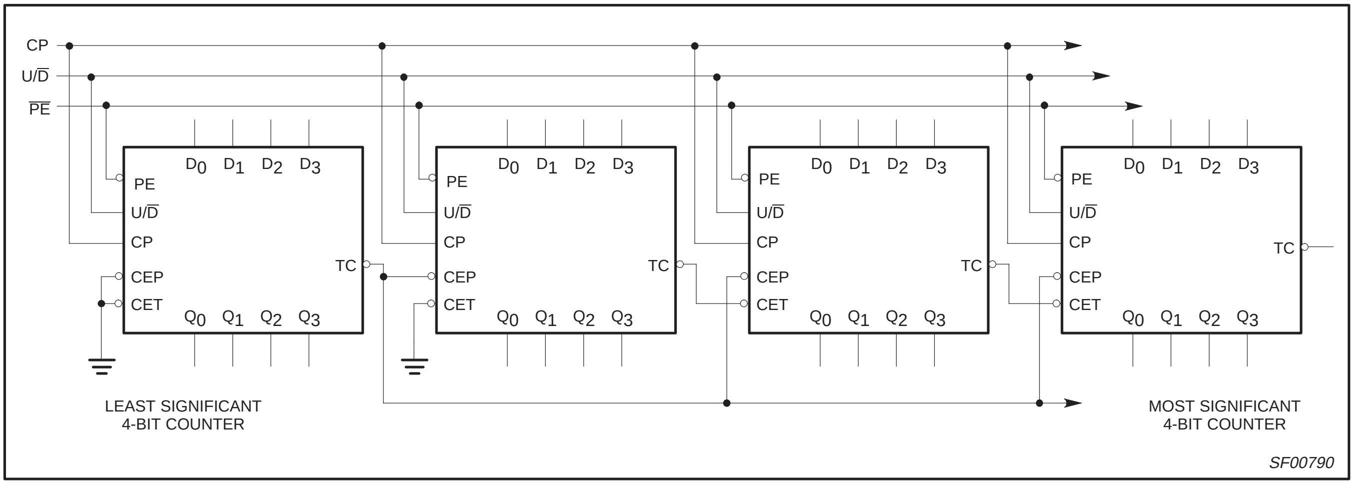


Typical timing sequence: reset outputs to zero; preset to binary twelve; count to thirteen, fourteen, fifteen, zero, one, and two; inhibit

LOGIC DIAGRAM



APPLICATION



Synchronous multistage counting scheme

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CC}	DC supply voltage (for max. speed performance)		2.7	3.6	V
	DC supply voltage (for low-voltage applications)		1.2	3.6	
V_I	DC input voltage range		0	5.5	V
V_O	DC output voltage range		0	V_{CC}	V
T_{amb}	Operating free-air temperature range		–40	+85	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.2 to 2.7V V_{CC} = 2.7 to 3.6V	0 0	20 10	ns/V

ABSOLUTE MAXIMUM RATINGS[1]

In accordance with the Absolute Maximum Rating System (IEC 134)
Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +6.5	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage	Note 2	–0.5 to +5.5	V
I_{OK}	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	± 50	mA
V_O	DC output voltage	Note 2	–0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current	V_O = 0 to V_{CC}	± 50	mA
I_{GND}, I_{CC}	DC V_{CC} or GND current		± 100	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	 above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 500 500	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP[1]	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2V	V_{CC}			V
		V_{CC} = 2.7 to 3.6V	2.0			
V_{IL}	LOW level Input voltage	V_{CC} = 1.2V			GND	V
		V_{CC} = 2.7 to 3.6V			0.8	
V_{OH}	HIGH level output voltage	V_{CC} = 2.7V; V_I = V_{IH} or V_{IL}; I_O = –12mA	V_{CC} – 0.5			V
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = –100µA	V_{CC} – 0.2	V_{CC}		
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = –12mA	V_{CC} – 0.6			
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = –24mA	V_{CC} – 1.0			
V_{OL}	LOW level output voltage	V_{CC} = 2.7V; V_I = V_{IH} or V_{IL}; I_O = 12mA			0.40	V
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = 100µA		GND	0.20	
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = 24mA			0.55	
I_I	Input leakage current	V_{CC} = 3.6V; V_I = 5.5V or GND		±0.1	±5	µA
I_{CC}	Quiescent supply current	V_{CC} = 3.6V; V_I = V_{CC} or GND; I_O = 0		0.1	10	µA
ΔI_{CC}	Additional quiescent supply current per input pin	V_{CC} = 2.7V to 3.6V; V_I = V_{CC} –0.6V; I_O = 0		5	500	µA

NOTES:

1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC CHARACTERISTICS

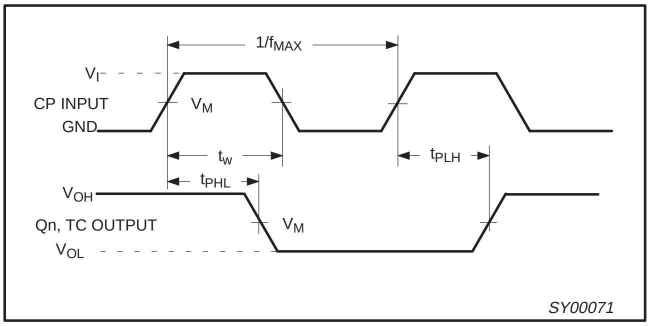
GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF; $R_L = 500\Omega$; $T_{amb} = -40°C$ to $+85°C$

SYMBOL	PARAMETER	WAVEFORM	LIMITS						UNIT
			V_{CC} = 3.3V ±0.3V			V_{CC} = 2.7V		V_{CC} = 1.2V	
			MIN.	TYP[1]	MAX.	MIN.	MAX.	TYP	
t_{PHL}/t_{PLH}	propagation delay CP to Q_n	1	-	5.0	8.5	-	9.5	24	ns
t_{PHL}/t_{PLH}	propagation delay CP to $\overline{TC}$	1	-	6.5	10.8	-	12.8	30	ns
t_{PHL}/t_{PLH}	propagation delay $\overline{CET}$ to $\overline{TC}$	2	-	5.3	8.7	-	9.7	19	ns
t_{PHL}/t_{PLH}	propagation delay U/$\overline{D}$ to $\overline{TC}$	4	-	5.7	9.5	-	10.5	24	ns
t_W	clock pulse width HIGH or LOW	1	4.0	1.2	-	5.0	-	-	ns
t_{su}	set-up time D_n to CP	3	2.5	1.0	-	3.0	-	-	ns
t_{su}	set-up time $\overline{PE}$ to CP	3	3.0	1.2	-	3.5	-	-	ns
t_{su}	set-up time U/$\overline{D}$ to CP	5	5.5	2.8	-	6.5	-	-	ns
t_{su}	set-up time $\overline{CEP}$, $\overline{CET}$ to CP	5	4.5	2.1	-	5.5	-	-	ns
t_h	hold time D_n, $\overline{PE}$, $\overline{CEP}$, $\overline{CET}$, U/$\overline{D}$ to CP	3 and 5	0	–2.5	-	0	-	-	ns
f_{max}	maximum clock pulse frequency	1	125	200	-	110	-	-	MHz

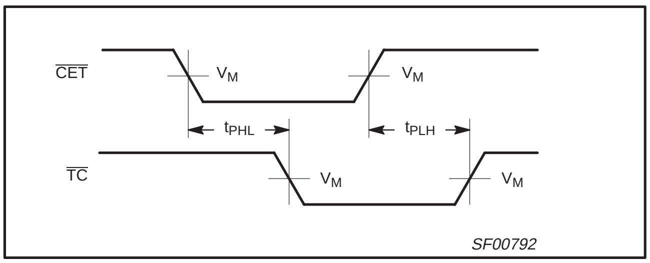
NOTE:
1. These typical values are measured at V_{CC} = 3.3V and T_{amb} = 25°C.

AC WAVEFORMS

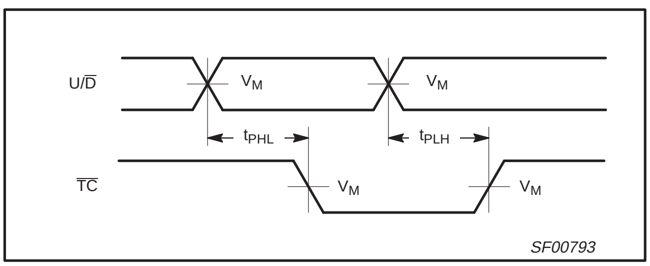
V_M = 1.5 V at $V_{CC} \geq$ 2.7 V
V_M = 0.5 • V_{CC} at V_{CC} < 2.7 V
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.



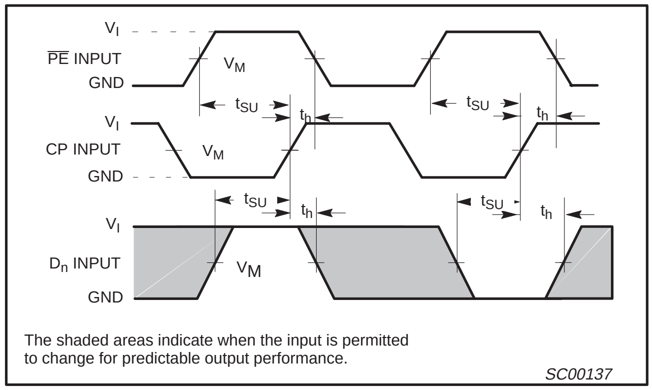
Waveform 1.   Clock (CP) to outputs (Q_n, TC) propagation delays, the clock pulse width and the maximum clock frequency.



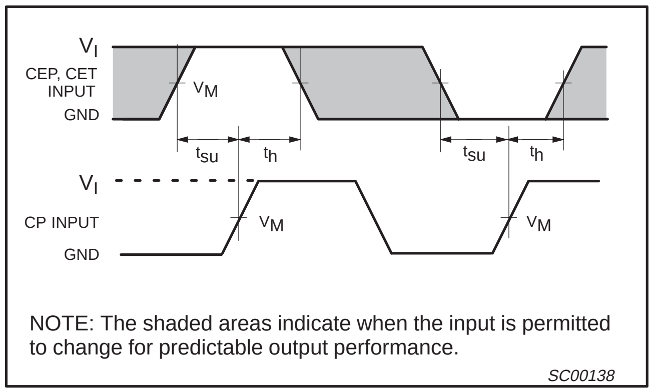
Waveform 2.   Input (CET) to output (TC) propagation delays and output transition times.



Waveform 3.   Master reset ($\overline{MR}$) pulse width, the master reset to output (Q_n, TC) propagation delays and the master reset to clock (CP) removal times.

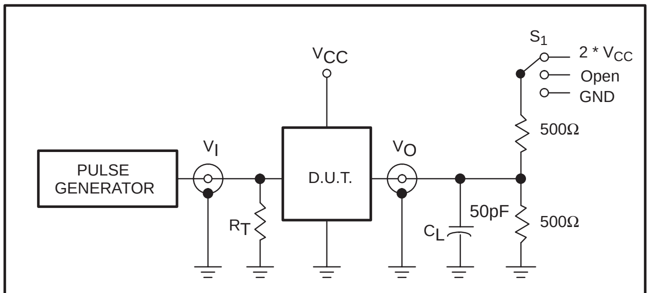


Waveform 4.   Setup and hold times for the input (D_n) and parallel enable input ($\overline{PE}$).



Waveform 5.   CEP and CET setup and hold times.

TEST CIRCUIT



SWITCH POSITION

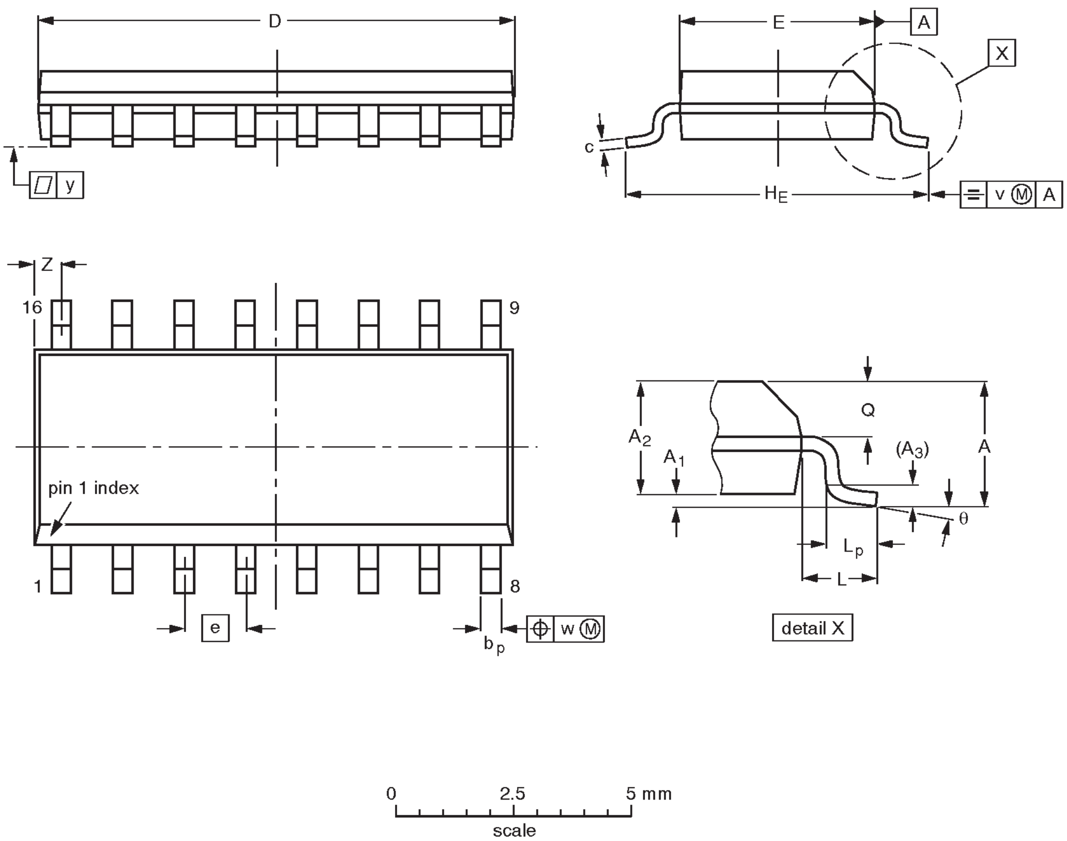
TEST	S_1
t_{PLH}/t_{PHL}	Open

V_{CC}	V_I
< 2.7V	V_{CC}
2.7–3.6V	2.7V

SV00903

Waveform 6.   Load circuitry for switching times.

SO16: plastic small outline package; 16 leads; body width 3.9 mm SOT109-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

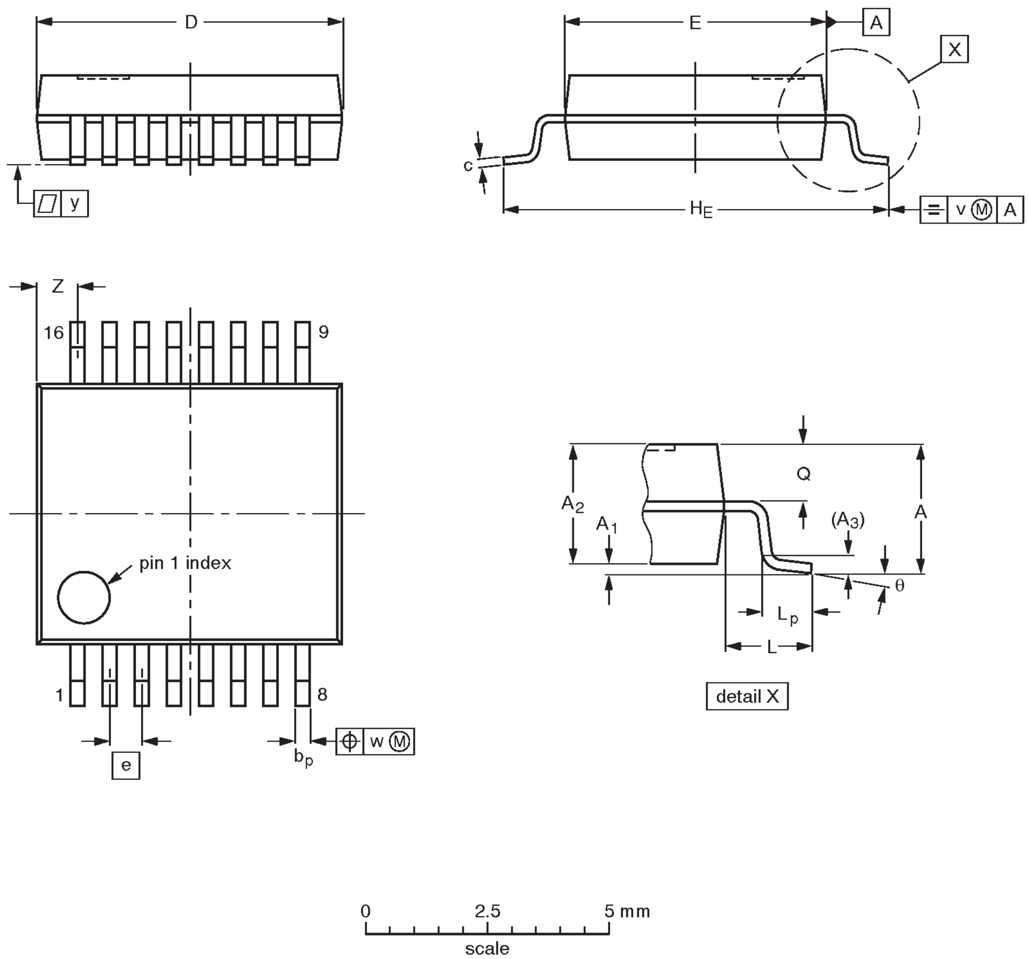
UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.0098 0.0039	0.057 0.049	0.01	0.019 0.014	0.0098 0.0075	0.39 0.38	0.16 0.15	0.050	0.24 0.23	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT109-1	076E07S	MS-012AC				~~91-08-13~~ 95-01-23

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm SOT338-1



DIMENSIONS (mm are the original dimensions)

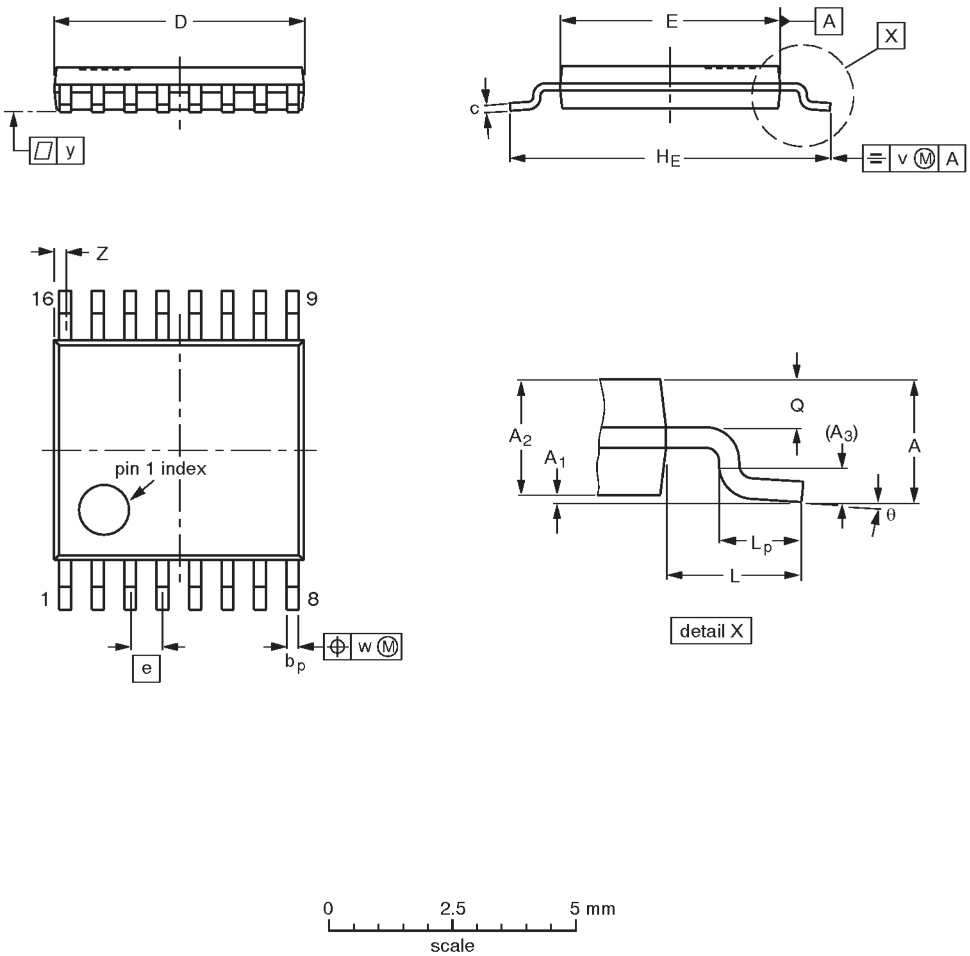
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.00 0.55	8° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT338-1		MO-150AC				~~94-01-14~~ 95-02-04

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm SOT403-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D [(1)]	E [(2)]	e	H_E	L	L_p	Q	v	w	y	Z [(1)]	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT403-1		MO-153				~~94-07-12~~ 95-04-04

NOTES

DEFINITIONS

Data Sheet Identification	Product Status	Definition
Objective Specification	Formative or in Design	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
Preliminary Specification	Preproduction Product	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product Specification	Full Production	This data sheet contains Final Specifications. Philips Semiconductors reserves the right to make changes at any time without notice, in order to improve design and supply the best possible product.

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