UPC. EETAC. Bachelor Degree. 2A. Digital Circuits and Systems (CSD). F. J. Robert, J. Jordana. Grades will be available on April 12. Questions about the exam: office time.

Exam 1 **April 5, 2019**

Problem 1. (Option A) **2.5p**

Given de following logic function: Y = *f*(a, b, c, d) = a·b + c'+ a·c·d

a) Express the function using only 2-input NAND. Draw the equivalent logic circuit.
b) Express the function as a product of maxterms and represent its truth table.
c) Implement the logic function with the method of decoders (MoD).
d) Implement the logic function with the method of multiplexers (MoM) and a MUX4.

Problem 1. (Option B) **2.5p**

a) Deduce the equation that exactly corresponds to the circuit Q = *f*(S1, S0, A, B) represented in Fig. 1.
b) Deduce the circuit's truth table using Boole's Algebra.
c) If the circuit's logic gates are LS-TTL technology, with a propagation delay of 10 ns, calculate the maximum speed of computing.

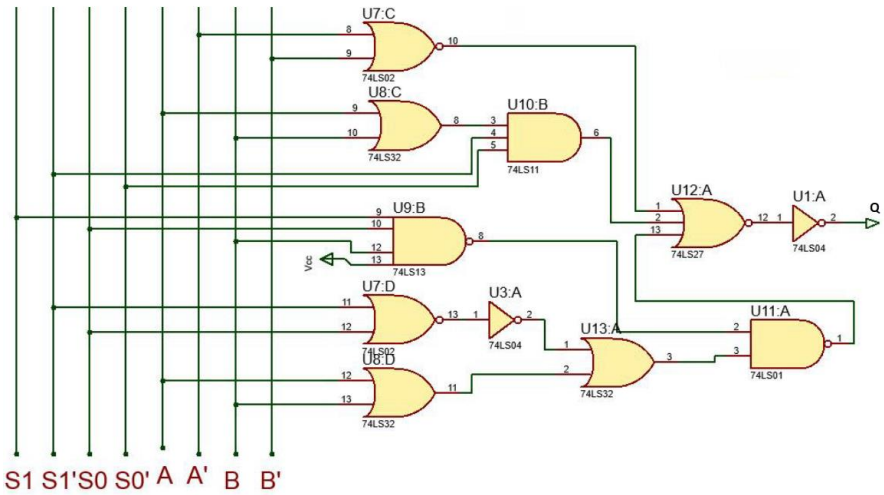


Fig. 1
Combinational circuit based on logic gates.

Problem 2. **2.5p**

In the Fig. 2 there is the RTL view of a synthesized circuit obtained with Quartus II in the target chip Cyclone III.

a) Justify if it is a flat or a hierarchical design. How many VHDL files the project contains?
b) Draw the symbol of the top entity, naming all the input and output ports.
c) Draw the truth table of the top entity and indicate how many minterms and maxterms has the output **Y**.
d) Draw the architecture of this top entity using the plan A (equations) and represent the logic circuit.

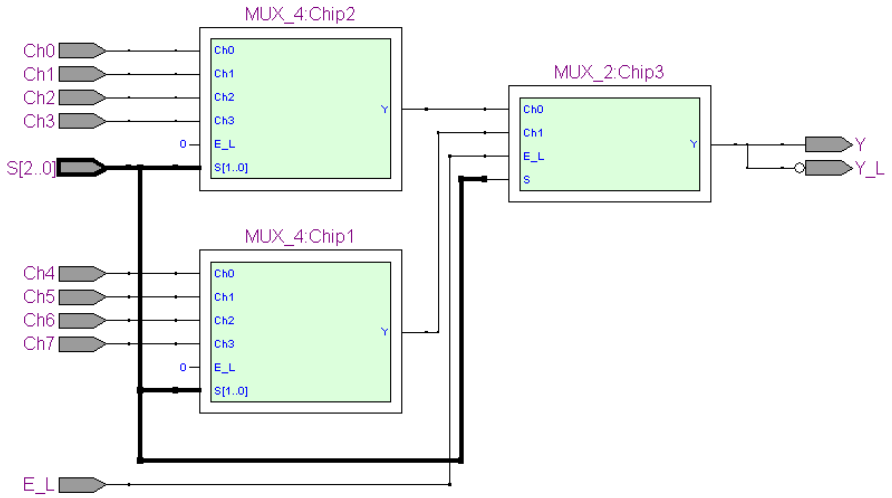


Fig. 2
RTL view from the EDA synthesizer tool.

Target chip Cyclone III. 3C16F484C6N

Problem 3. **2.5p**

The Fig. 3 represents a timing diagram for a functional simulation of the *Integer_comp_8bit* comparator when **N** = 0 and so, the data is unsigned in radix 2.

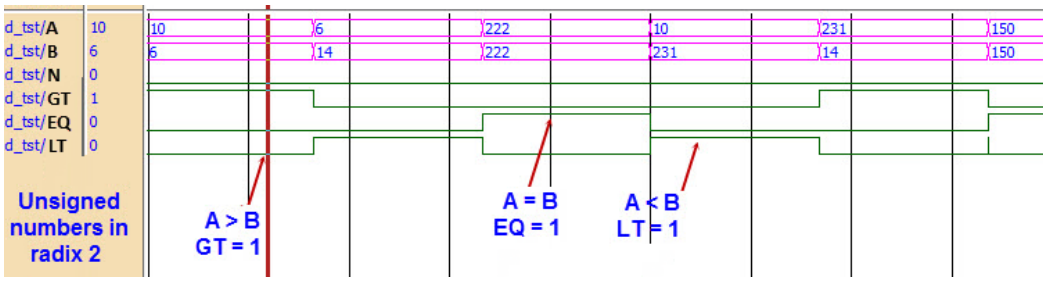
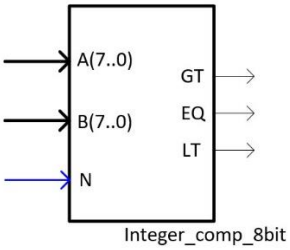


Fig. 3
Timing diagram of a functional simulation for the circuit represented below:



a) Draw some values of the truth table of the circuit calculating the outputs for the input stimulus in Fig. 3.
b) Represent a similar timing diagram deducing the outputs suposing that now the same **A** and **B** input combinations in '0' and '1' represents data in signed decimal (two's complement) and **N** = '1'.
c) Propose a hierarchical internal design of the circuit in Fig. 3 based on simpler chips of the same kind.
d) Explain how does the *Comp_1bit* works (truth table) and how many maxterms has its output GT.

Problem 4. **2.5p**

The Fig. 4 shows the symbol of an 8-bit adder/substractor which operates two's complemented data.

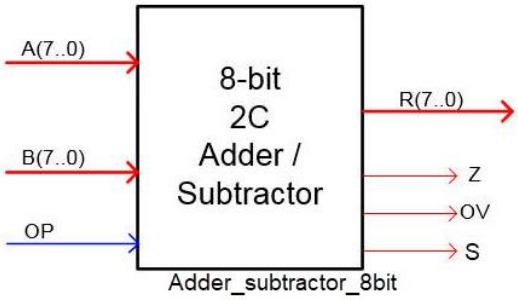


Fig. 4
Symbol for the *Adder_subtractor_8bit*

a) Indicate the binary combinations and their equivalent signed decimal results of the following operations. Indicate as well the value of the flags Z, OV and S.
   a. A = 01010101, B = 01110011, OP = 0
   b. A = 01010101, B = 01110011, OP = 1
   c. A = 10101111, B = 01111100, OP = 0
b) Invent an internal architecture of this circuit based in plan C2 (hierarchical). Indicate component names, chip references and signals involved.
c) Which condition has to be met in order to detect overflow (OV)? Which is the way to solve it using gates?
d) Accordingly to the results from the gate-level simulation presented in the Fig. 5, calculate the maximum speed of operation of the *Adder_Subtractor_8bit* and the propagation delay of a single gate for this technological implementation.

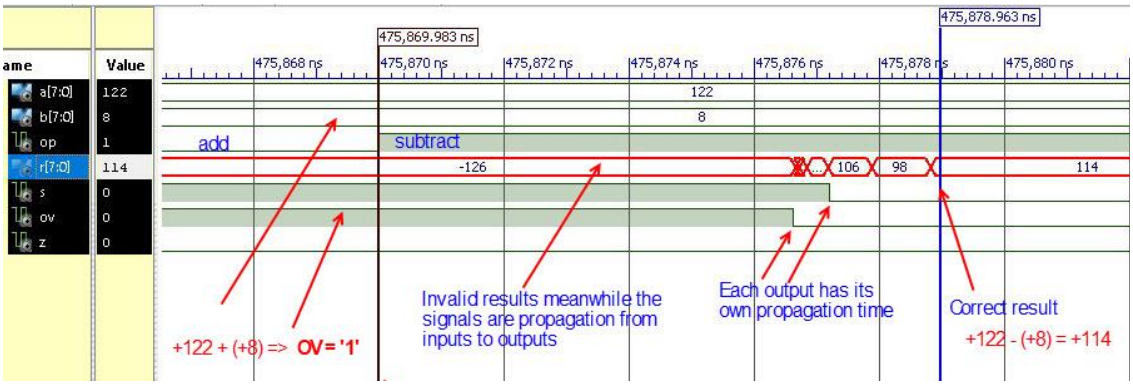


Fig. 5
Example of gate-level simulation and analysis of the 8-bit adder and subtractor in a given signal transition.