UPC. EETAC. Bachelor Degree. 2A. Digital Circuits and Systems (CSD). Grades will be available online by April 19th. Questions about the exam at office time.

Midterm exam. **April 12th, 2023**

Problem 1 (4p)

1. Design the function Q in Fig. 1 using only 2-input NOR. Explain firstly your plan.

$$Q = f(P_3, P_2, P_1, P_0) = \sum m(1,2,4,6,7,12,15) + \sum d(0,10,11)$$

Fig. 1. Truth table of *Circuit_Q*. ('*d*' terms are do not care).

2. *Circuit_Q* invented in **1** will be implemented using a classic technology HCT (High Speed CMOS with TTL outputs) with the electrical characteristics shown in Fig. 2. Deduce and explain the maximum speed of computing and estimate the total power consumption at such frequency. What is the minimum value of *Min_Pulse* if we intent to run gate-level simulations?

Symbol	Parameter	Test Conditions V_{CC} = 5 V	T_A = -40°C to +85°C		Unit
			Min	Max	
V_{IH}	High-level Input Voltage		2.0		V
V_{IL}	Low-level Input Voltage			0.8	V
V_{OH}	High-level Output Voltage	I_{OH} = -20µA	4.4		V
		I_{OH} = -4mA	3.84		
V_{OL}	Low-level Output Voltage	I_{OL} = 20µA		0.1	V
		I_{OL} = 4.0mA		0.33	
I_{CC}	Supply Current	V_I = GND or V_{CC}		20	µA

Power Dissipation Capacitance per Gate	Typ	Unit
C_L	12	pF

Symbol	Parameter	Typ	Unit
t_{Pg}	Propagation Delay	12	ns

$$P_{gate} = P_S + P_{dyn} = I_{CCQ} \cdot V_{CC} + V_{CC}^2 \cdot C_L \cdot f$$

Fig. 2. Technology characteristics of HCT logic gates (adapted from 74HCT00 datasheet).

3. Firstly, invent *Circuit_Q* using the method of multiplexers (MoM) with a *MUX_4*. Secondly, solve the *MUX_4* expanding *MUX_2* and logic if necessary. How many VHDL files will this project contain?

4. Firstly, invent *Circuit_Q* using the method of decoders (MoD). Secondly, solve your decoder expanding *Dec_3_8* and logic if necessary.

Problem 2 (3p)

1. The truth table in Fig. 3 represents some inputs and outputs of a *Selectable_Add_Subt_Comp_11bit* arithmetic circuit for operating with both integer (N = 1) and radix-2 (N = 0) numbers. Integers can be added (OP = 0) and subtracted (OP = 1). Radix-2 numbers can only be added. Draw its symbol. Find the range of input and output data and complete the truth table with the given values converting firstly the numbers into binary.

N	OP	A	B	C_{out}	R	OV	Z	GT	EQ	LT
0	x	666	1544	1	162	x	0	0	0	1
0	x	1544	1544							
0	x	1544	666							
0	x	0	0	0	0	x	1	0	1	0
1	0	(+1018)	(-555)	x	(+463)	0	0	1	0	0
1	1	(-1018)	(-1018)							
1	1	(-1018)	(+1018)							
1	0	(+666)	(-1018)							
1	1	(-1018)	(-666)							

Fig. 3. Truth table of the arithmetic circuit *Selectable_Add_Subt_Comp_11bit.*

2. Draw an example of timing diagram (use the Fig. 4 template). Supposing *Min_Pulse* = 74.2 µs calculate how long does it take to test all the truth table of *Selectable_Add_Subt_Comp_11bit*.

3. Design the *Selectable_Add_Subt_Comp_11bit* circuit using components.

4. Propose an internal circuit for the *Int_Add_Subt_11bit* using components.

5. Draw the truth table of an *Adder_1bit*. Design an *Adder_4bit* using *Adder_1bit.*

6. Implement the output Z using logic gates.

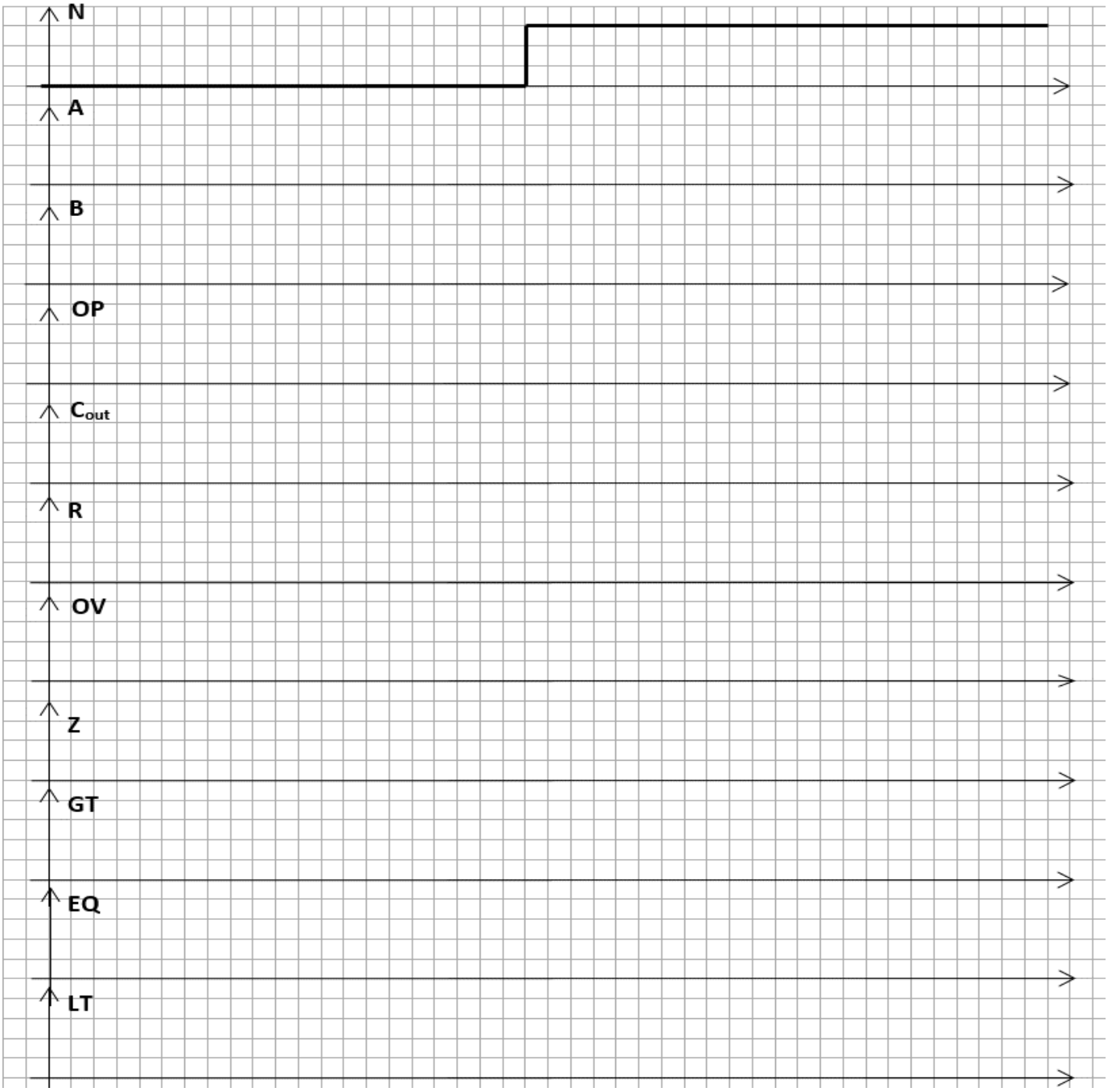

Fig. 4. Waveform template for representing the timing diagram in question **2**.

Problem 3 (3p)

1. Analyse the *Circuit_Z* shown in Fig. 5 as Z = *f*(S1, S0, A, B) explaining firstly your method.

2. Calculate the limiting resistor to drive an active-low LED (V_{AKQ} = 1.8 V, I_{DQ} = 3.9 mA) connected at the output Z supposing the electrical characteristics in Fig. 2. (Draw the circuit first).

3. Invent *Circuit_Z* drawing a flowchart or schematic using plan B. Translate the main details to VHDL.

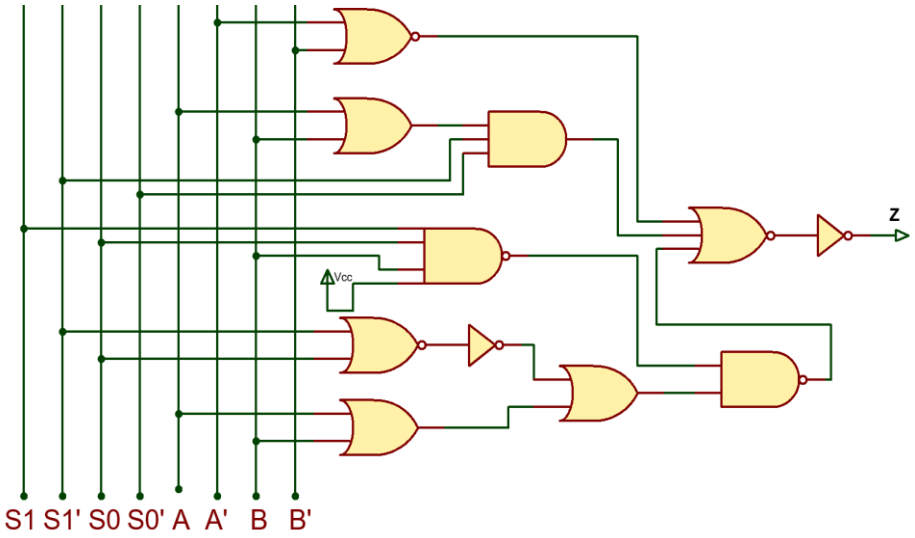

Fig. 5 *Circuit_Z* based on logic gates.