# Problem 1

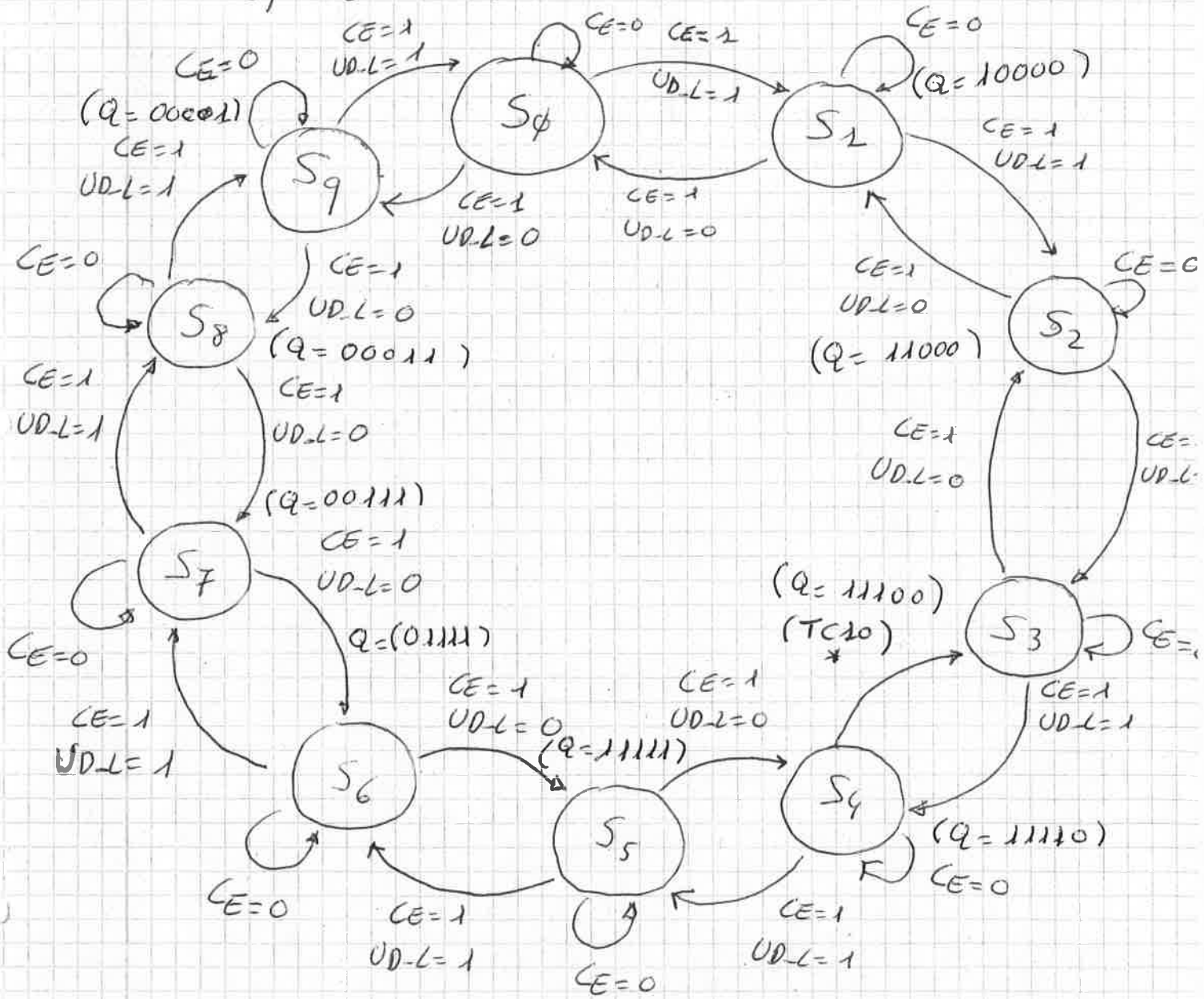
a)

| | $Q_4$ | $Q_3$ | $Q_2$ | $Q_1$ | $Q_0$ |
|---|---|---|---|---|---|
| $S_\phi$ | 0 | 0 | 0 | 0 | 0 |
| $S_1$ | 1 | 0 | 0 | 0 | 0 |
| $S_2$ | 1 | 1 | 0 | 0 | 0 |
| $S_3$ | 1 | 1 | 1 | 0 | 0 |
| $S_4$ | 1 | 1 | 1 | 1 | 0 |
| $S_5$ | 1 | 1 | 1 | 1 | 1 |
| $S_6$ | 0 | 1 | 1 | 1 | 1 |
| $S_7$ | 0 | 0 | 1 | 1 | 1 |
| $S_8$ | 0 | 0 | 0 | 1 | 1 |
| $S_9$ | 0 | 0 | 0 | 0 | 1 |

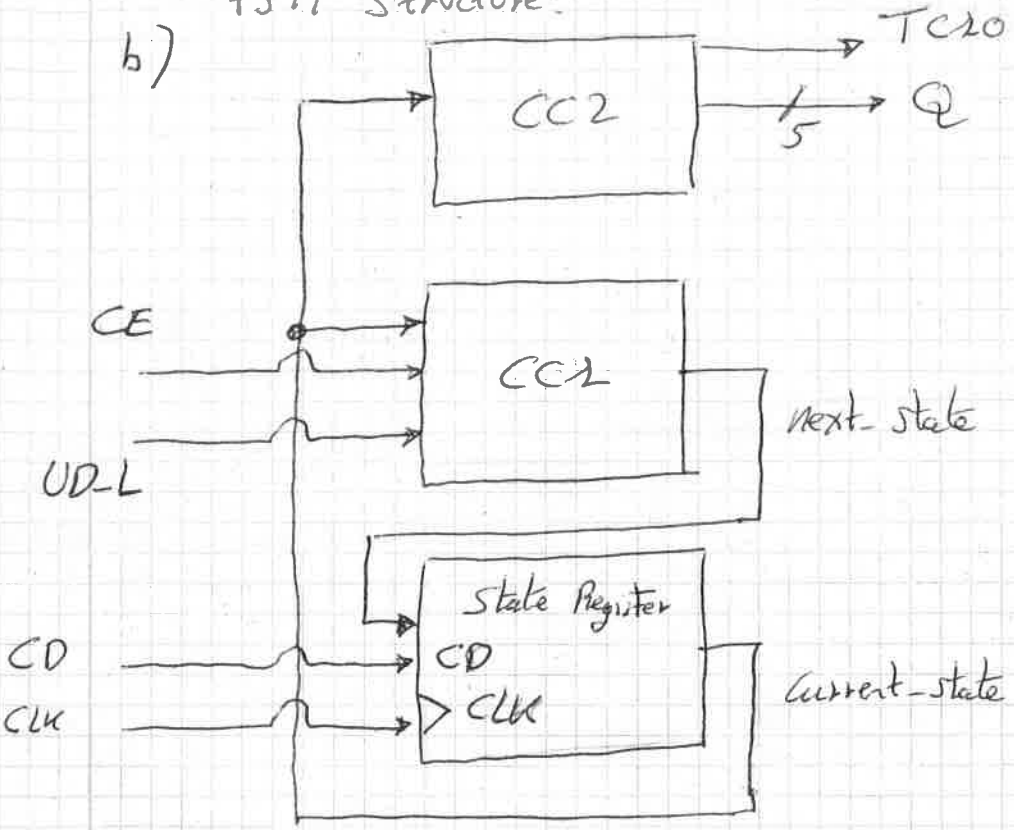
TC10 (*)

TC10 = 1 in S9 and Up and CE = 1

or in S0 and Down and CE = 1



b) FSM structure:

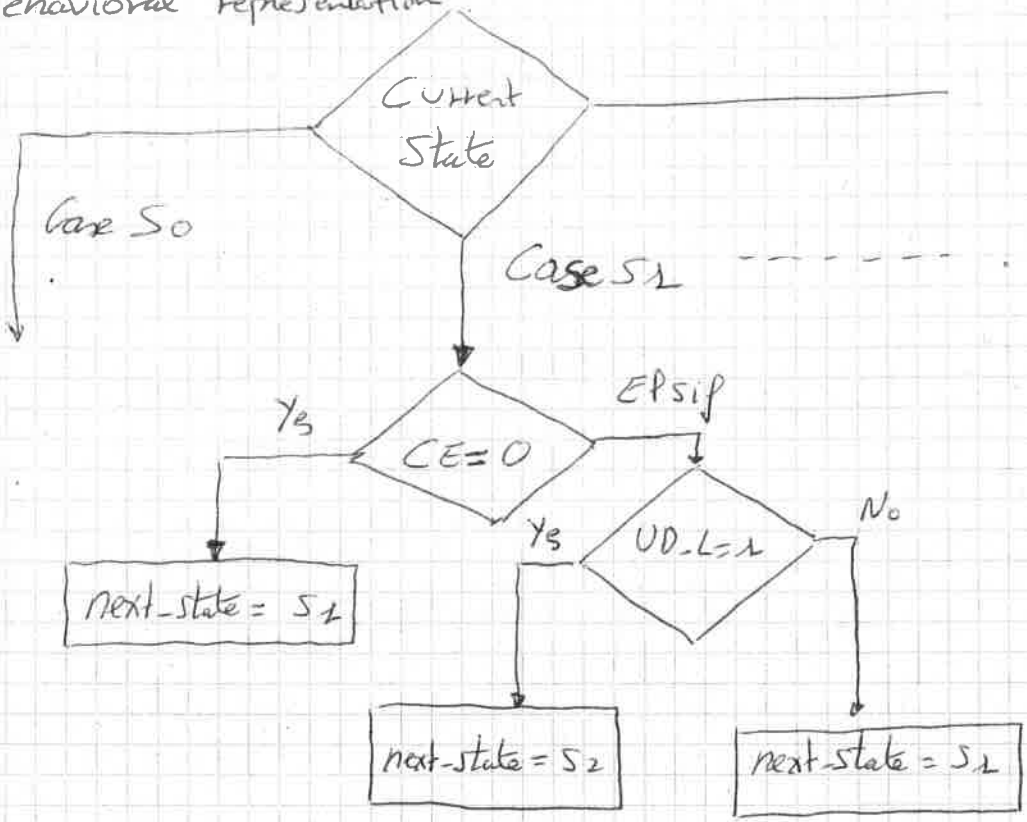



There are 10 states, then if coded in one-hot it is required 10 D-FF and if coded in binary it is required 4 D-FF.

c)

| CE | UD_L | current_state | next_state |
|---|---|---|---|
| 0 | X | $S_0$ | $S_0$ |
| 1 | 1 | $S_0$ | $S_1$ |
| 1 | 0 | $S_0$ | $S_9$ |
| 0 | X | $S_1$ | $S_1$ |
| 1 | 1 | $S_1$ | $S_2$ |
| 1 | 0 | $S_1$ | $S_0$ |
| 0 | X | $S_2$ | $S_2$ |
| 1 | 1 | $S_2$ | $S_3$ |
| 1 | 0 | $S_2$ | $S_1$ |
| ⋮ | ⋮ | ⋮ | ⋮ |
| 0 | X | $S_9$ | $S_9$ |
| 1 | 1 | $S_9$ | $S_0$ |
| 1 | 0 | $S_9$ | $S_8$ |

Behavioral representation




d) Main VHDL sentences of CC2.

```
CC2: Process ( current_state, CE) UD_L )
    BEGIN
      If ((current_state = S9 ) AND (CE= '1') AND (UD_L=1))
          OR (current_state = S0) AND (CE='1') AND (UD-L=0)  Then
           TC10<='1';
      ELSE
           TC10 <='0';
      END IF

      CASE current_state is
            When S0 =>
                 Q <= "00000";
            when S1 =>
                 Q <= "10000";
            when S2 =>
                 Q <= "11000";
                 .
                 .
                 .
            when S9 =>
                 Q <= "00001";
    END CASE
    END PROCESS
```

e) The functional simulation is ideal
In this case the maximum frequency can be $\infty$

f)

$$f_{max} = \frac{1}{t_{CO} + N \cdot t_{PD}}$$

If CC2 has three levels of gate

$$f_{max} = \frac{1}{4'6ns + 3 \cdot 1'7ns} = \boxed{203'09\ MHz}$$