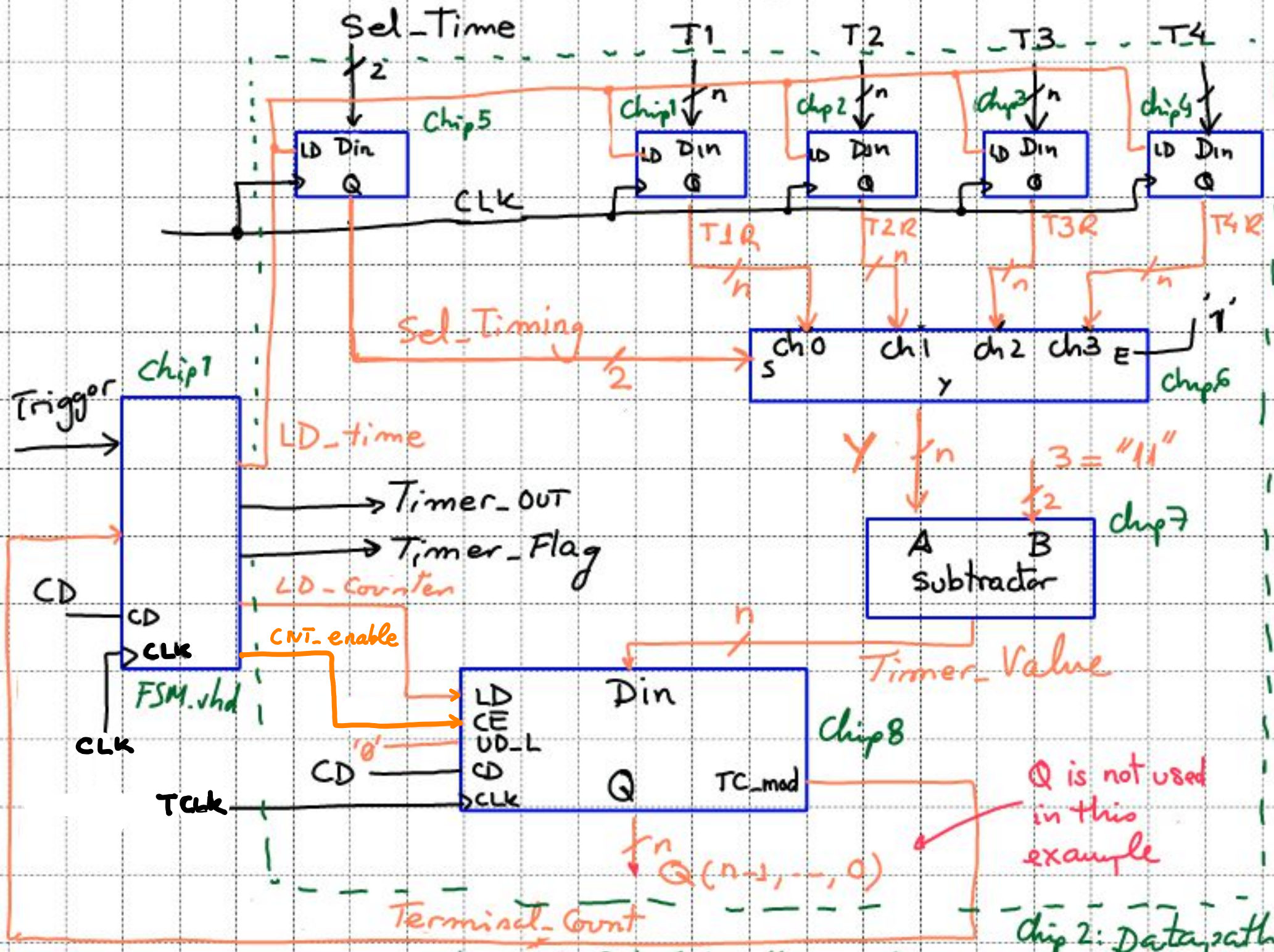
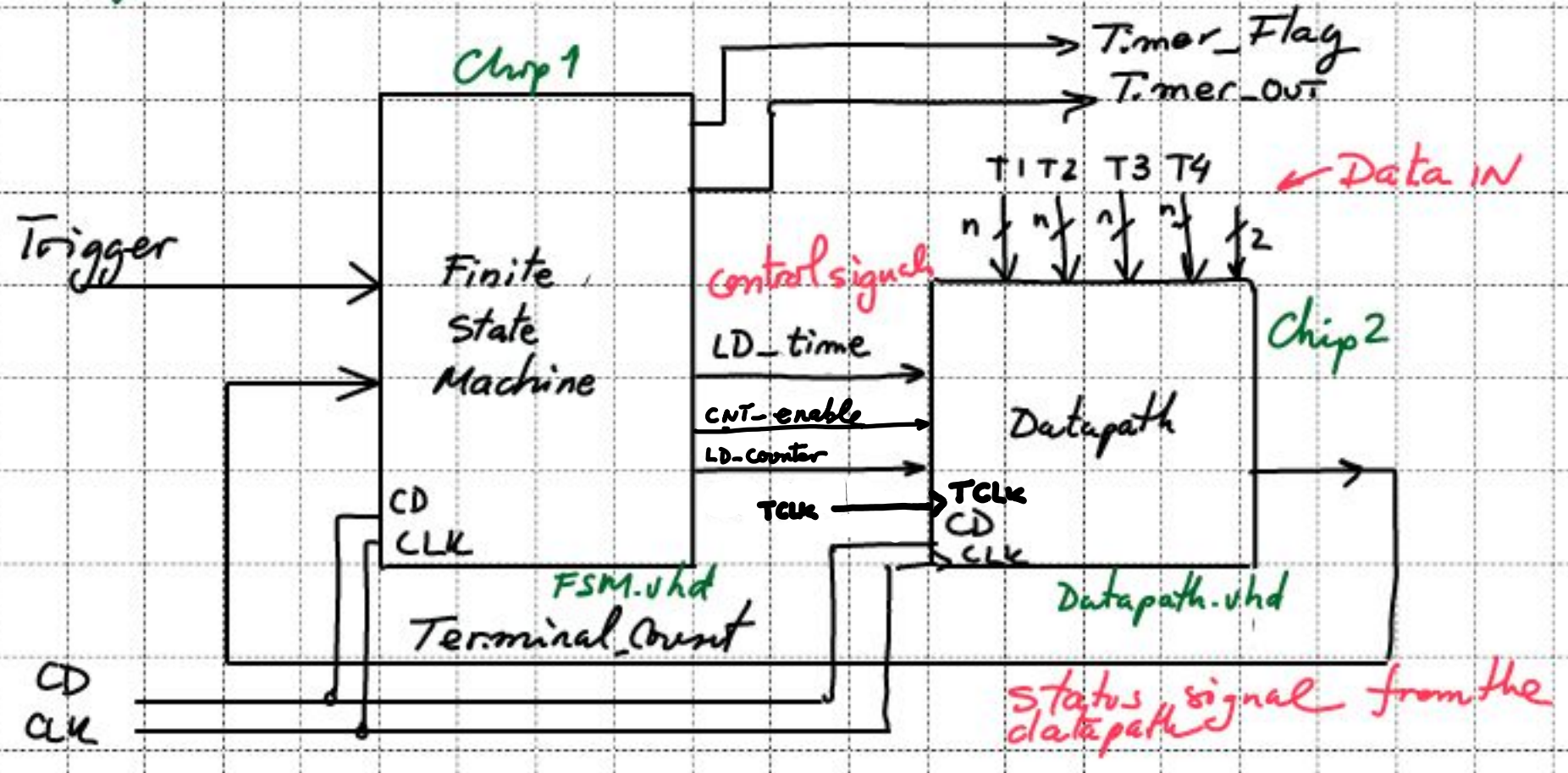
Let's consider an internal architecture

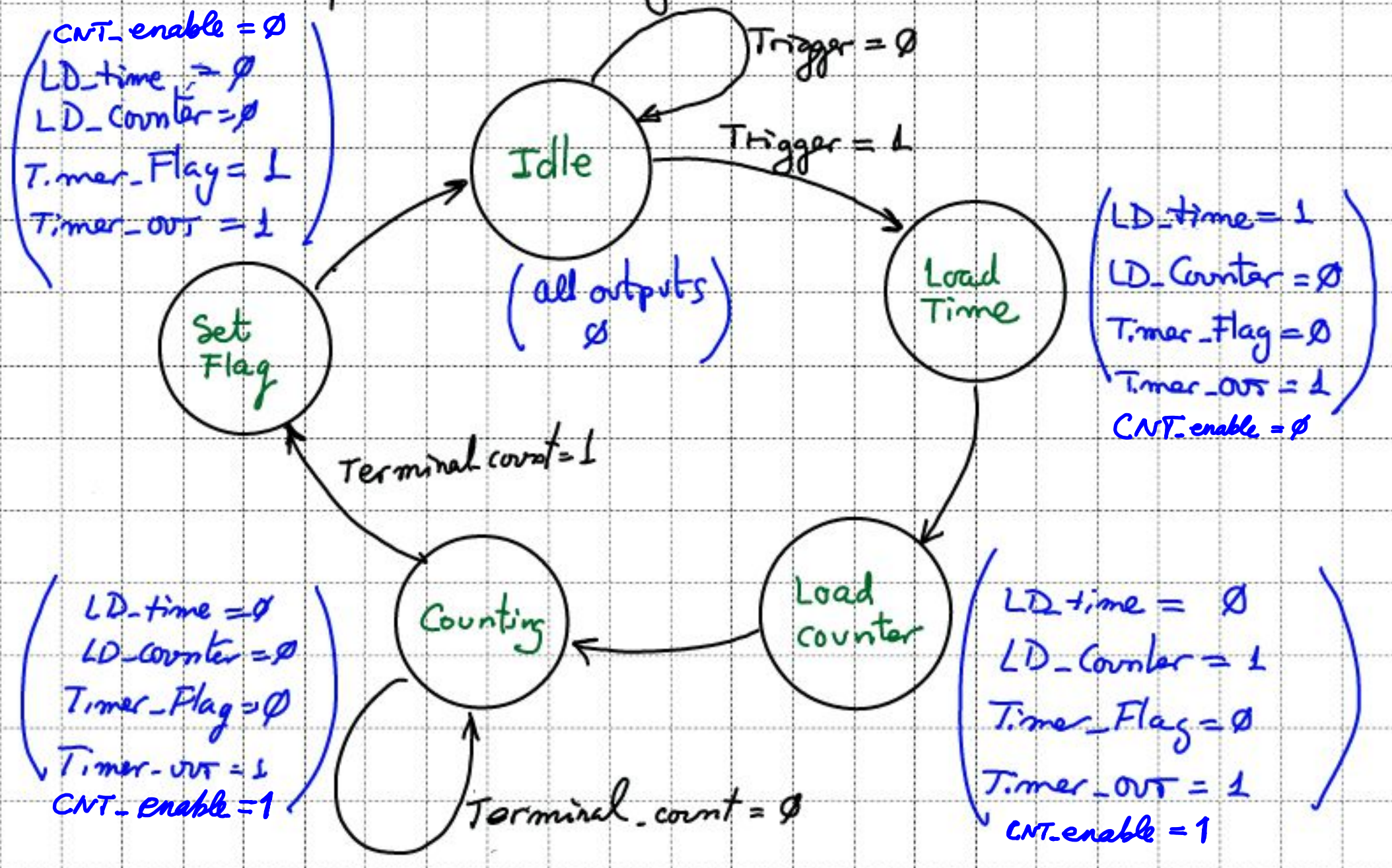


Chip 1 ... Chip 4 → Data_register_8bit, (Chip 5 the same)
Chip 6 → Octuple_MUX4 ; Chip 7 (adder optional); Chip 8 Counter 8bit

The internal programmable timer structure: a dedicated processor (Control Unit + Datapath)

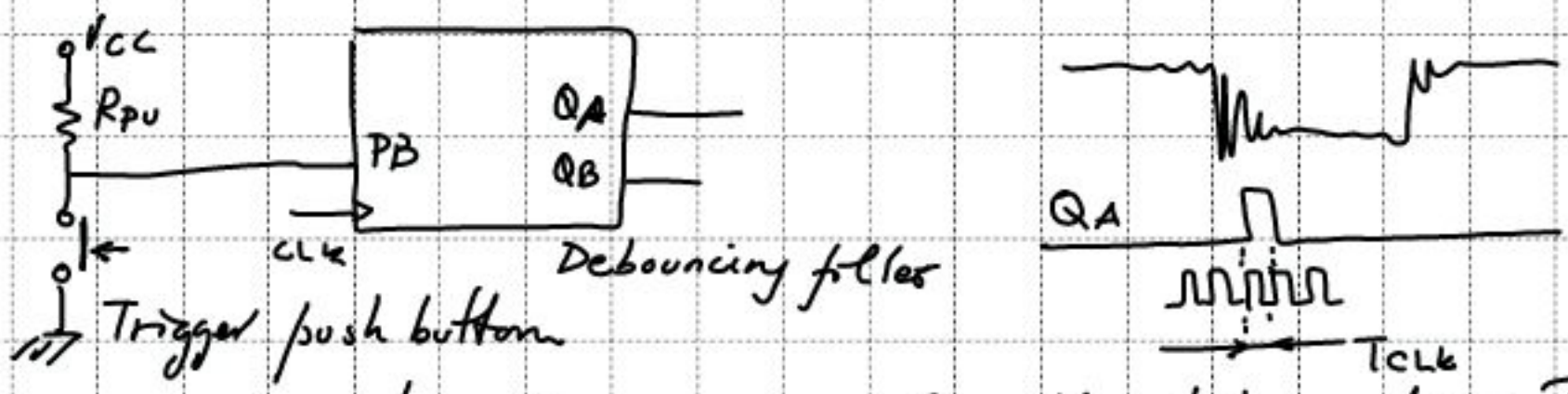


This is an example of state diagram to control the datapath and to generate the outputs :



Trigger has to be an input with a minimum duration of T_{CLK} and a maximum duration $T \cdot T_{CLK}$, because if not, it cannot be sampled correctly or <u>retrigger</u> the timer because when the timing period end the signal is yet active.

⇒ <u>Better</u> generate a synchronous 1 CLK pulse from a debouncing circuit. (see the tutorial in P6)



- How to prevent retriggering modifying the <u>state machine</u> ?