UPC. EETAC. Bachelor Degree. 2A. Digital Circuits and Systems (CSD). Dr F. J. Robert. Grades will be available online on January 28th. Questions about the exam at office time.

Exam 2. **January 22nd, 2021**

Problem 1. (2.5p)

Analyse the circuit represented in Fig. 1.

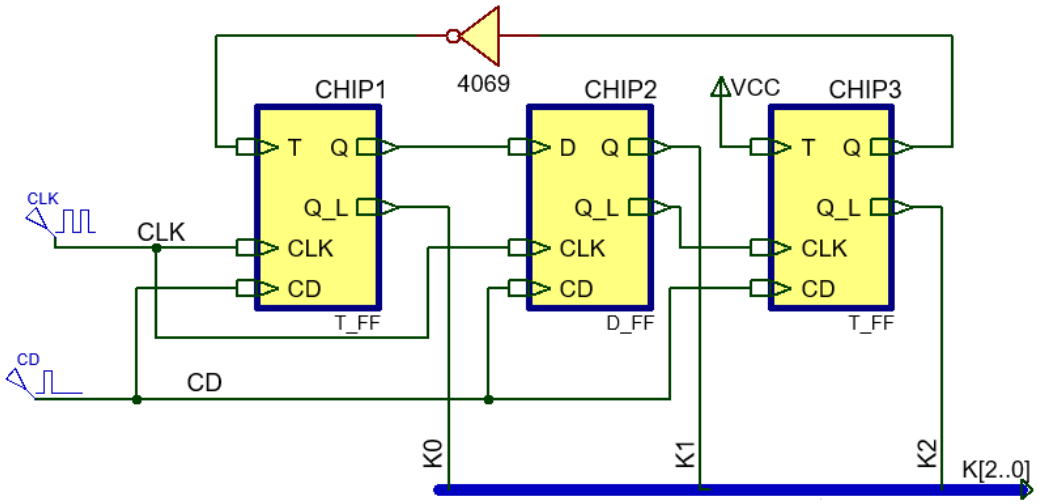


Fig. 1
Circuit based on 1-bit memory cells and logic gates.

a) Determine whether this circuit is synchronous or asynchronous and why.

b) How many VHDL files are necessary to develop and simulate the circuit using EDA tools?

c) Determine the output vector **K[2..0]** drawing a timing diagram considering enough CLK periods. Write down the binary codes generated.

d) If the *T_FF* component is planned as a standard FSM using *one-hot* state enumeration, how many *D_FF* are necessary in its state register?

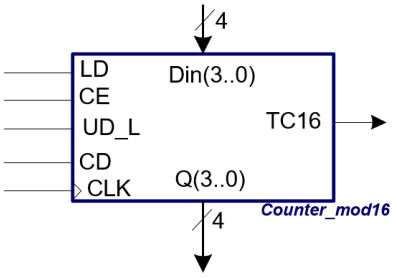
Problem 2. (3.5p)

Design (specify and plan) the programmable *Post_scaler* available in TMR2 represented in Fig. 2 using VHDL techniques and structural plan C2 for a target FPGA chip. Use standard sequential and combinational circuits and logic gates. Let us rename the symbol and ports: TMR2 is the **CLK** input to the circuit, T2OUTPS(3..0) is the frequency division selector **Div**(3..0), and Set TMR2IF output is the terminal count **TC**.

The *Post_scaler* can divide from 1:1 to 1:16 depending on Div(3..0) binary value from "0000" to "1111". For instance, if F_{CLK} = 15 kHz and Div(3..0) = "0100", the circuit becomes a 1:5 frequency divider generating F_{TC} = 3 kHz; if F_{CLK} = 84 MHz and Div(3..0) = "1011", the circuit becomes a 1:12 frequency divider generating F_{TC} = 7 MHz.

a)

Fig. 2. a) TMR2 postscaler block schematic from Microchip and our adapted symbol.



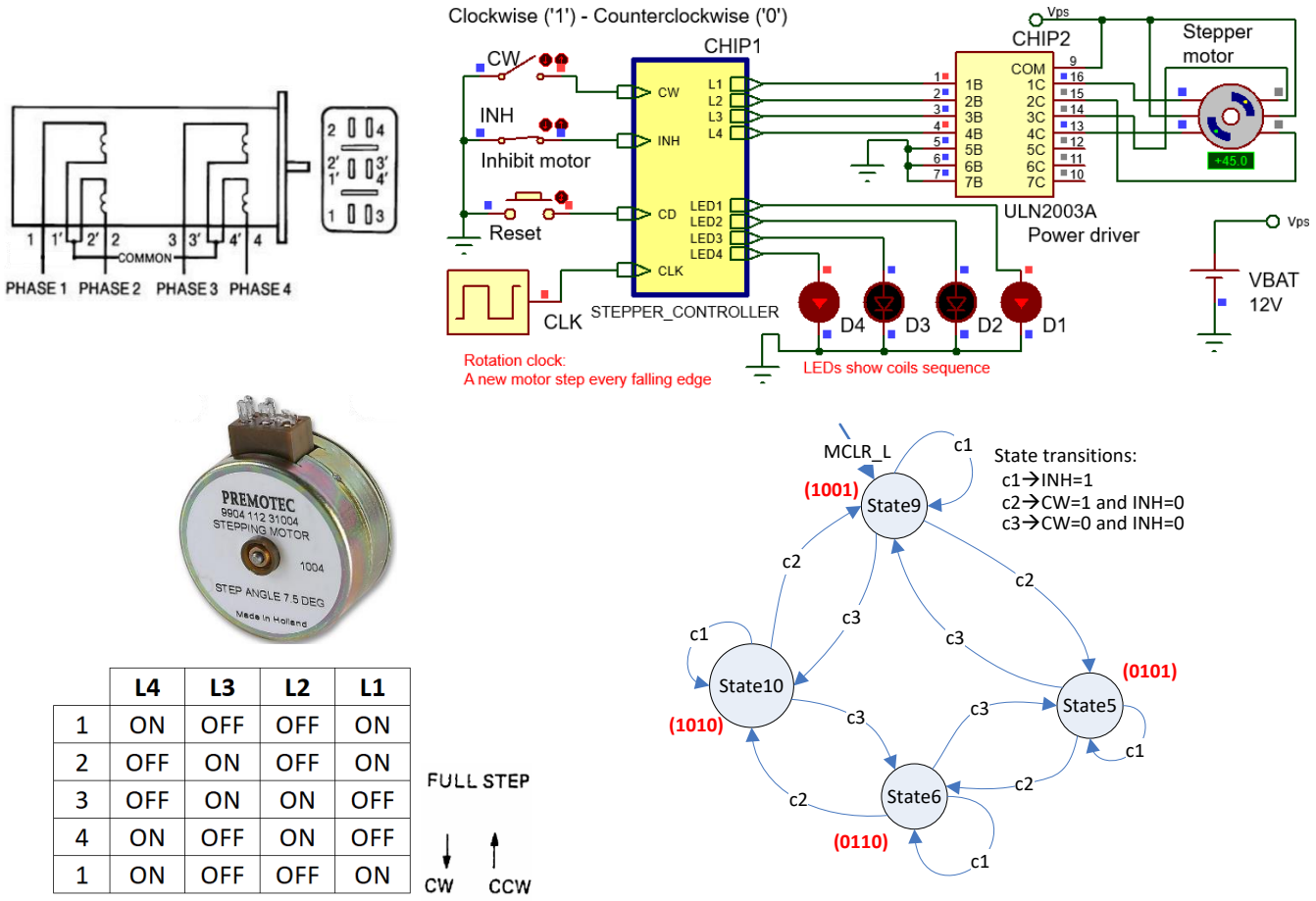
LD	CE	UD_L	Q^+	
1	x	x	Din	parellel load
0	0	x	Q	do nothing
0	1	1	$(Q+1)_2$	up (mod16)
0	1	0	$(Q-1)_2$	down (mod16)

b)

b) Symbol and function table of component *Counter_mod16* that may be used in this structural design.

Problem 3. (4p)

Design the digital control unit (*stepper_controller*) for the "9904 112 31004" stepping motor from Premotec shown in Fig. 3 following our microcontroller-based strategy. Today stepper motors can be found in computer peripherals, machine tools, medical equipment, automotive devices, or small business machines, to name a few applications. Clockwise (**CW**) and counter-clockwise (CCW) rotation can be achieved by reversing the step sequence. Inhibit (**INH**) is like a count disable, do not letting the motor rotate. Step or stride angle is 7.5 degree, thus 48 **CLK** periods are required for a full revolution. External CLK frequency is 96 Hz, and so when running it rotates at 2 revolutions per second. The idea is to connect four port pins to the motor coils and drive them with the right sequence so that the motor inhibits or rotates clockwise or counter-clockwise accordingly to the input signals INH and CW. Four additional pins are used connected to LED to visualise the coils binary sequence.



	L4	L3	L2	L1
1	ON	OFF	OFF	ON
2	OFF	ON	OFF	ON
3	OFF	ON	ON	OFF
4	ON	OFF	ON	OFF
1	ON	OFF	OFF	ON

Fig. 3 Example of two-phase stepper motor: characteristics, connections, full wave steeping sequence and unipolar winding circuit using a power driver to energise coils. Proposed state diagram to control the FSM.

1. Draw the schematic: input switches, outputs, reset (MCLR_L) and 4.8 MHz quartz crystal oscillator OSC.
2. Draw the hardware-software diagram. Why the rotation CLK block has to be connected to RB0/INT pin? What the interrupt service routine *ISR()* is used for?
3. Organise and name RAM variables for the project. Explain how to configure port pins and interrupts in *init_system*().
4. Explain how to poll the input values using bitwise operations in *read_inputs()*.
5. Explain how to drive the eight outputs using bitwise operations in *write_outputs()*.
6. Draw the truth table and flowchart for the *output_logic()*.
7. Draw the truth table and flowchart for the *state_logic()*.
8. Replace external CLK configuring TMR0 (in 8-bit mode) to obtain the same 96 Hz step frequency.

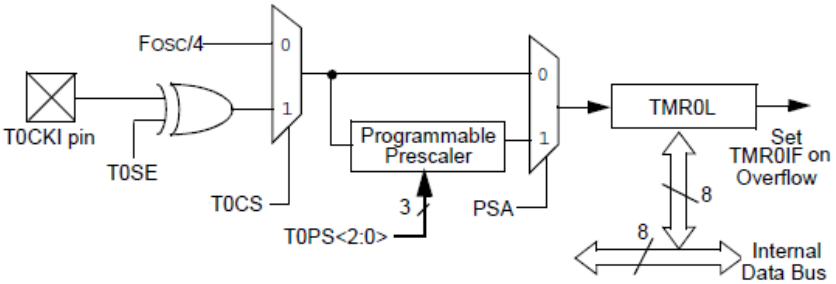


Fig. 4 TMR0 schematic in 8-bit mode.

UPC. EETAC. Bachelor Degree. 2A. Digital Circuits and Systems (CSD). Dr F. J. Robert. Grades will be available online on January 28th. Questions about the exam at office time.

Exam 2. **January 22nd, 2021**