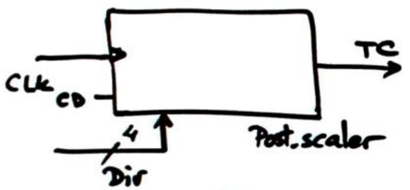
PROBLEM 2: This is a solution using Counter_mod16 as an up counter, MUX_16 and logic. Similar circuits can be inferred using Counter_mod16 as a down counter.

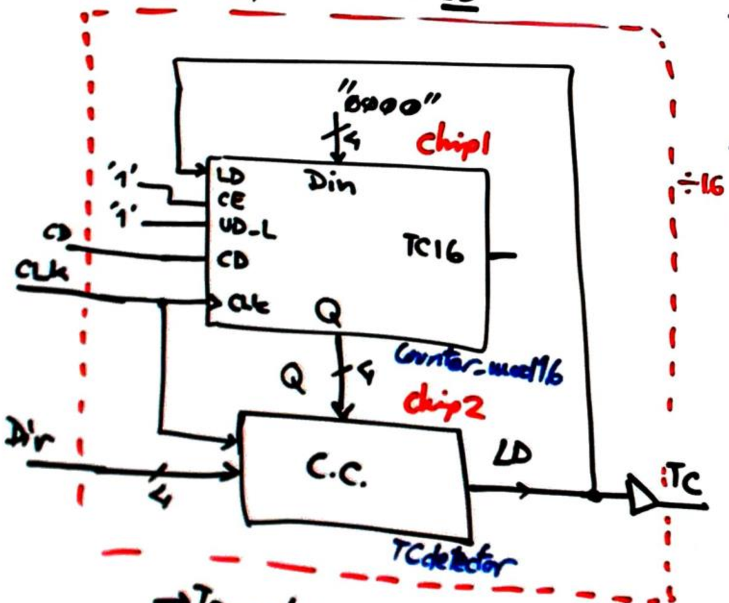


Dir = 0 → ÷1
Dir = 1 → ÷2
Dir = 2 → ÷3
⋮
Dir = 15 → ÷16

$F_{TC} = \frac{T_{CLK}}{16}$

Planning using a counter up

→ Counter_mod16 with parallel load LD



→ Truncated count when LD = 1 ↓ next state is Din = 0

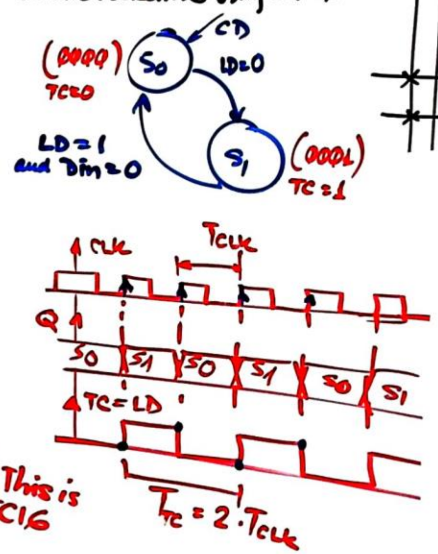
LD is programmable depending on Dir

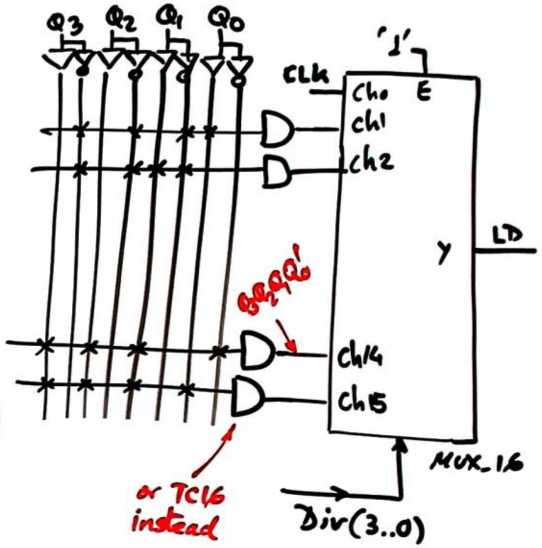
TC detector combinational circuit truth table

	Div	Q	CLK	LD (TC)
÷1	0000	x	CLK	CLK
÷2	0001	0001	x	1
	0001	any other	x	Ø
÷3	0010	0010	x	1
		any other	x	Ø
		⋮		
÷16	1111	1111	x	1
	1111	any other state	x	Ø

This is also TC16

channel selection using a MUX





→ We can design this table using logic gates or using components such MUX_16

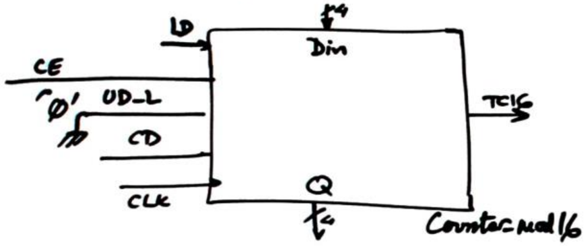
Using logic gates →

The circuit has 16 product terms

$LD = Div_3' \cdot Div_2' \cdot Div_1' \cdot Div_0' \cdot Q_3' \cdot Q_2' Q_1' Q_0' \cdot CLK +$

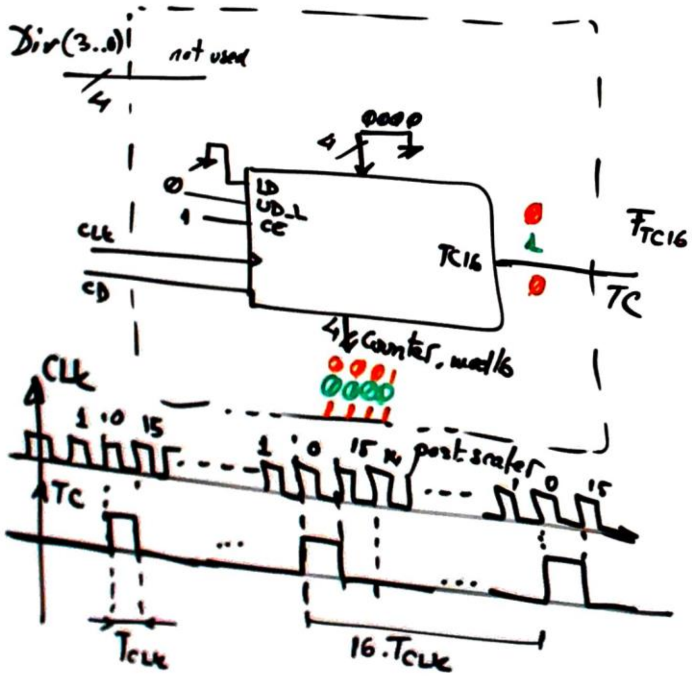
$+ Div_3' \cdot Div_2' \cdot Div_1' \cdot Div_0 \cdot Q_3' Q_2' Q_1' Q_0 + \dots$

alternative design using a down counter block



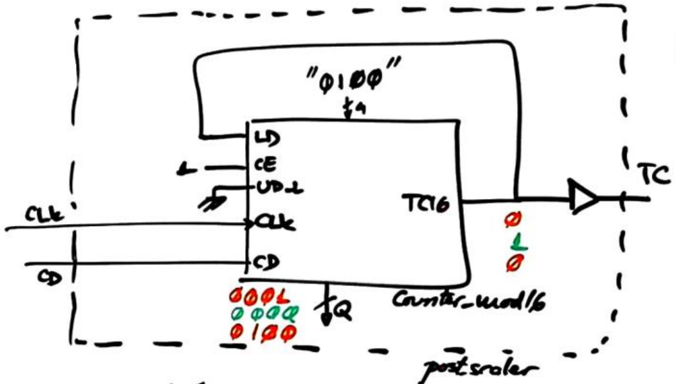
TC16 = 1 when UD_L = Ø and CE = 1
and Q = "ØØØØ"

* If LD = 'Ø' → the circuit Counter_mod16 is a fixed $\frac{1}{16}$ frequency divider



$F_{TC16} = \frac{F_{CLK}}{16}$

*If Din = "Ø1ØØ"
LD = TC16



The system goes counting down and when Q = ØØØØ → TC16 = 1
→ LD = 1 ⇒ Q^+ = Ø1ØØ,
and so, it is a ÷5 frequency divider

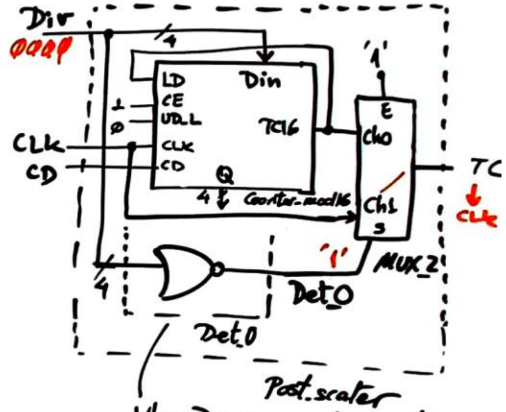
⇒ In this way, it is clear that
Div = Din ⇒ Programmable frequency divider

Div = Ø1ØØ → ÷5
Div = Ø1Ø1 → ÷6
⋮
Div = 1111 → ÷16

and so, Div = ØØØ1 → ÷2

→ What about ÷1 when Div = ØØØØ?
TC = CLK

*Final circuit

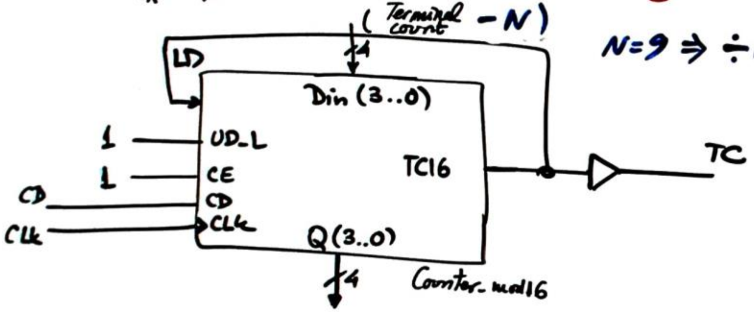


When Div(3..0) = "ØØØØ"
Det_0 → '1' →
Select Ch1 → TC = CLK
÷1

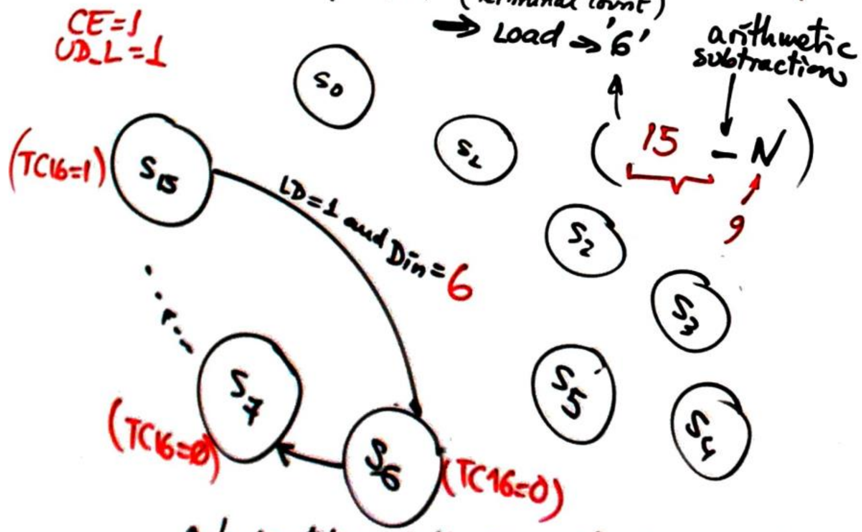
When Div(3..0) ≠ "ØØØØ"
Det0 → 'Ø'
Select Ch0 → TC = TC16
⇒ programmable divider from ÷2 to ÷16

And yet, even another alternative way using an UP counter and replacing logic circuits (gates + MUX_16) by arithmetic blocks

* For instance: $\div 10$ to infer what algorithm to use

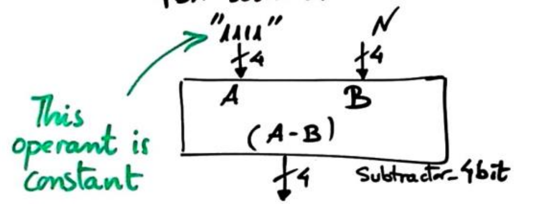


TC16 = 1 when CE=1 and UD_L=1 and Q=1111 (Terminal count) → Load → '6'

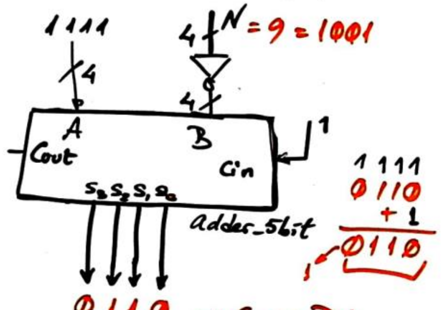


Only 10 states of the 16 available are used

* This arithmetic circuit is a 4bit subtractor



$A - B = A + (-B) = A + 2C(B)$



$$\begin{array}{r} 1111 \\ 0110 \\ +\ 1 \\ \hline 1\ 0110 \end{array}$$

0110 → 6 → Din

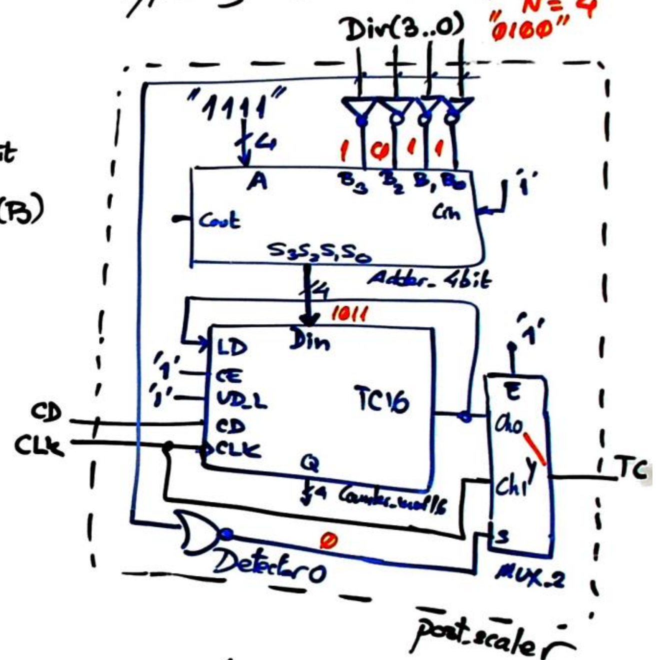
* N = 6 → 0110 → 1001

$$\begin{array}{r} 1111 \\ +\ 1001 \\ 1 \\ \hline 1\ 1001 \end{array}$$

→ Din = 9 (divider ÷7)

$S_9 \to S_{10} \to S_{11} \to S_{12} \to S_{13} \to S_{14} \to S_{15}$

* Thus, the final circuit must include a MUX_2 to detect N=0 → ÷1 for bypassing the Counter_mod16



$$\begin{array}{r} 1111 \\ +\ 1011 \\ 1 \\ \hline 1\ 1011 \end{array}$$

→ Din

States $S_{11} \to S_{12} \to S_{13} \to S_{14} \to S_{15}$

$\boxed{\div 5}$

$$\begin{array}{r} 1111 \\ +\ 0000 \\ 1 \\ \hline 1\ 0000 \end{array}$$ ← Div

→ Din → $\div 16$