UPC. EETAC bachelor's degrees in telecommunications systems and in network engineering. Semester 2A. Digital Circuits and Systems (CSD). Grades will be available online by June 27th. Questions about the exam at office time.

**Second exam.** **Solve 7 of the 10 questions** **June 20th, 2023**

Chapter 3 questions

**1.** Use the TMR0 in 16-bit mode of operation (shown in Fig. 2) for designing a frequency meter instrument for measuring unknown frequencies up to 5 MHz. The gate time $T_G$ = 50 ms, when the counter is enabled, is derived from an external signal. Discuss the specifications and propose a plan including hardware and software schematics and diagrams.

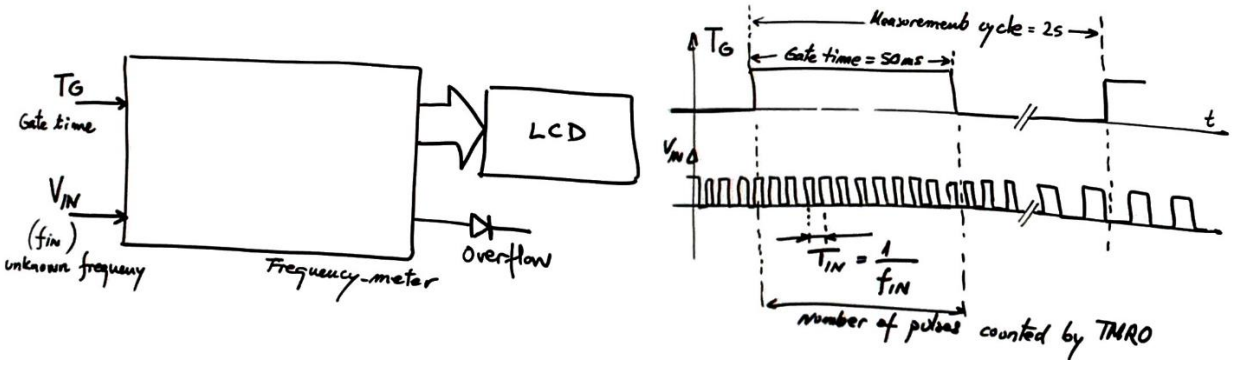



Fig. 1.

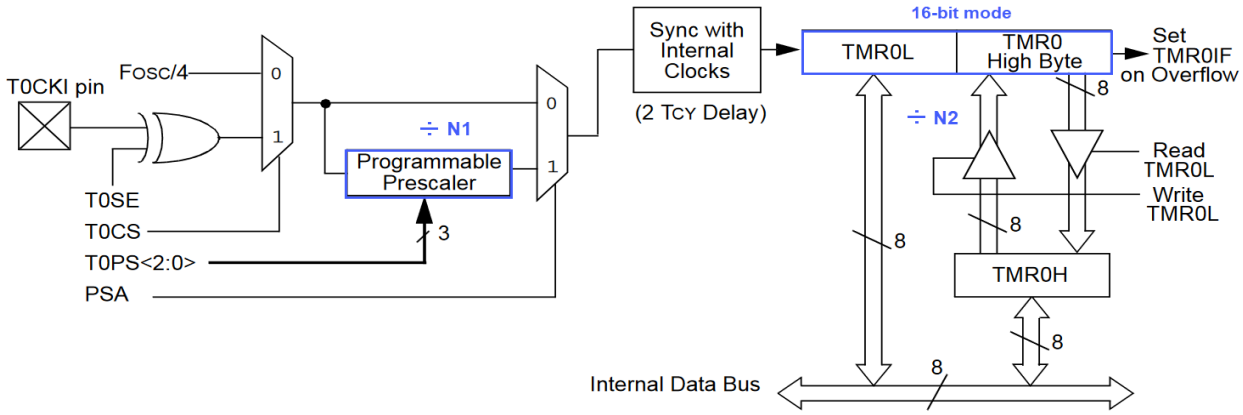



Fig. 2.

**2.** Add to the previous frequency meter an LCD display to show the measured frequency and messages to indicate overflow. Explain what hardware and software modifications are required.

**3.** Use TMR2 peripheral represented in Fig. 3 to replace the external gate time $T_G$ = 50 ms pulse in Fig. 1. Explain how to plan and organise the software and what functions are affected. $F_{OSC}$ = 12 MHz.

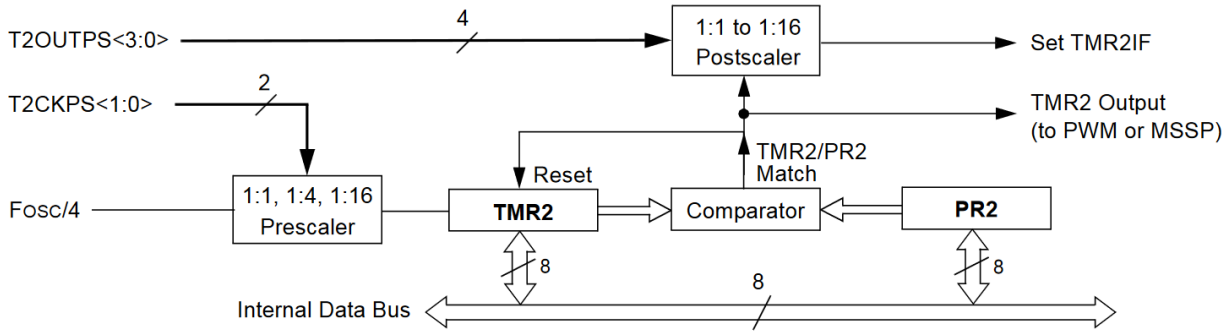



Fig. 3.

**4.** Read the pins display minutes (DM) and display seconds (DS) of the application represented in Fig. 4 connected at RC6 and RB3 respectively. Explain the flowchart and how are evolving variable content using bitwise operations. Draw and explain what is a power-on reset circuit and how does it work.

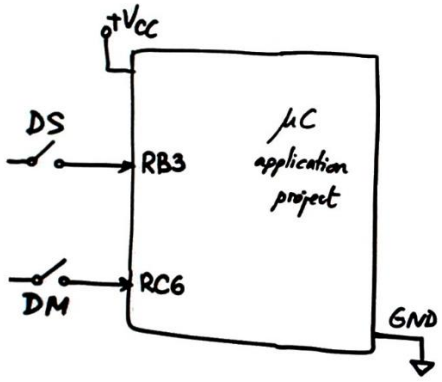



Fig. 4.

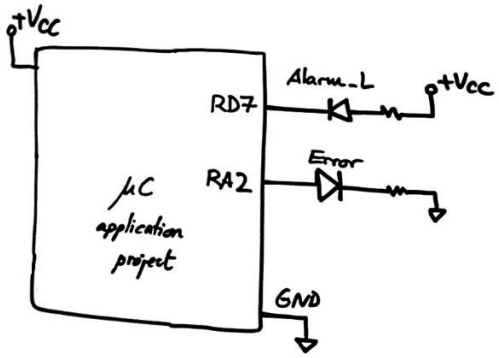
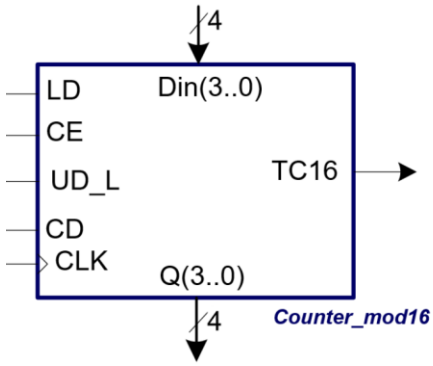



Fig. 5.

**5.** Write the variables *var_Alarm* and *var_Error* in the pins indicated in Fig. 5. Explain the flowchart of bitwise operations and the memory content while preserving the port bits of no interest. Draw and explain what is a typical circuit for a microcontroller oscillator and why it is required.

Chapter 2 questions

**6.** Invent a synchronous BCD down counter module 13 (*Counter_BCD_mod13*) using plan C2 and the universal component *Counter_mod16* the symbol of which is proposed in Fig. 6. Specifications (symbol, timing diagram, state diagram) and plan (schematics and components).

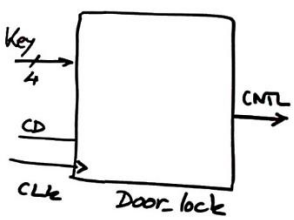



| LD | CE | UD_L | $Q^+$ | Synchronous operation after the CLK's rising edge |
|---|---|---|---|---|
| 1 | x | x | Din | Parallel load (register data) |
| 0 | 0 | x | Q | Do nothing (inhibit) |
| 0 | 1 | 1 | $(Q+1)_{mod16}$ | Up counting in binary |
| 0 | 1 | 0 | $(Q-1)_{mod16}$ | Down counting in binary |

TC16 = '**1**' when CE = '1' *and* [(Q = 15 *and* UD_L = '1') *or* (Q = 0 *and* UD_L = '0')]; '0' otherwise

Fig. 6.

**7.** Using our FSM or dedicated processor strategies, invent a digital door lock as represented in Fig. 7 that opens a door (CNTL = '1') only when the secret code "65" is detected. Specifications (symbol, timing diagram, state diagram) and plan. Determine the number of VHDL files required.



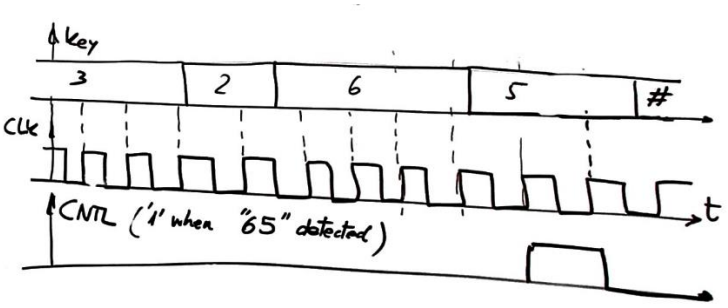




Fig. 7.

**8.** Invent the synchronous *CLK_generator* represented in Fig. 9. Specifications and plan. Number of *D_FF* used. Number of VHDL files included in the project. Design a *Freq_div_N* using plan Y.

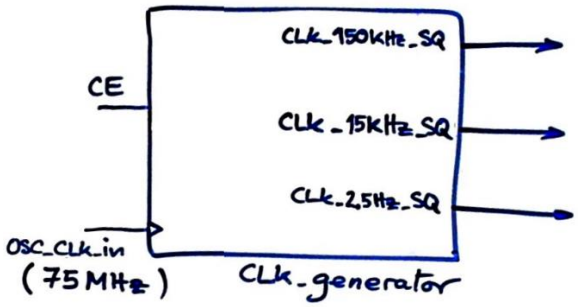
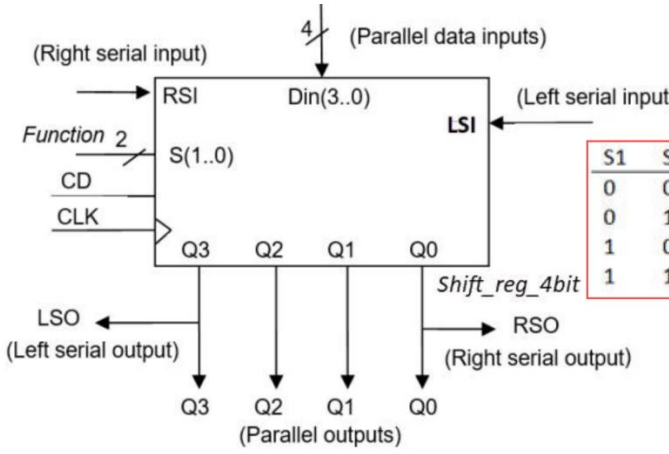



Fig. 8.

**9.** Invent a 10-bit universal shift register using plan C2 and the component represented in Fig. 9. Use the invented device to generate a 10-bit LED left rotator in one-hot code.




| S1 | S0 | Function |
|---|---|---|
| 0 | 0 | Do nothing (inhibit) |
| 0 | 1 | Shift right (Q3 ← RSI, Q2← Q3, Q1← Q2, Q0← Q1) |
| 1 | 0 | Shift left (Q0 ← LSI, Q1← Q0, Q2← Q1, Q3← Q2) |
| 1 | 1 | Parallel load data (Q ← Din) |

Fig. 9.

**10.** Analyse the circuit in Fig. 10 using a timing diagram and find the binary codes in the output vector Q(2..0). Discuss what will be the circuit's maximum frequency of operation, and how to measure it in the laboratory.

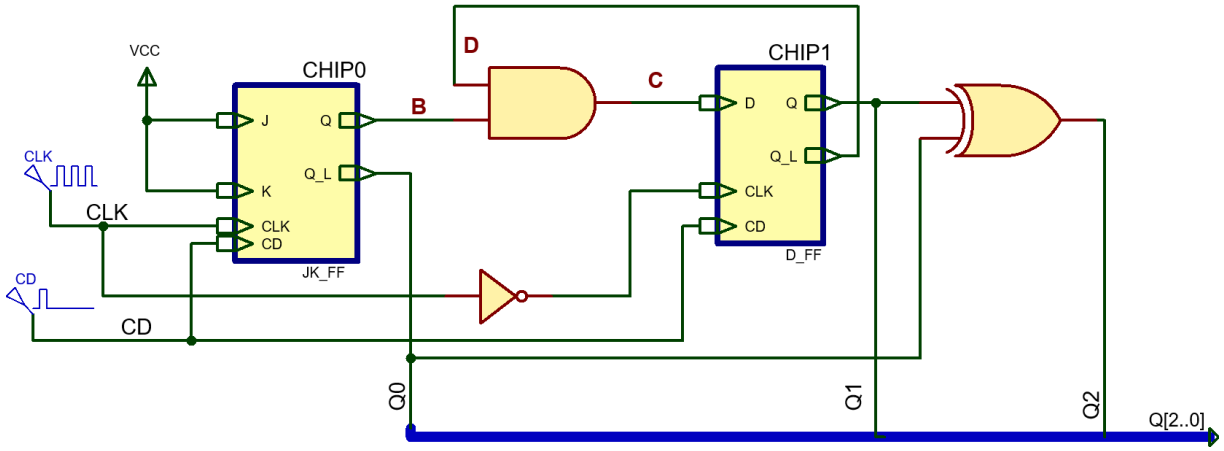



Fig. 10.