  

DIGITAL CIRCUITS AND SYSTEMS

# P\_Ch1: 10-bit 2C adder/subtractor

**Cooperative group**

TEAM NUMBER: \_\_\_\_GXX\_\_\_\_\_

DUE DATE: \_\_\_\_ **31/10/2017**\_\_\_\_\_\_\_\_\_ 1st review due date: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

STUDY TIME:

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Study time** **(in hours)**  | Group work | Classroom and laboratory sessions  |  | Sessions out of classroom  |  |
| Individual | Student 1 Student 2Student 3 |  |
|  |
|  |

STATEMENT:

My signature below indicates that I have (1) made equitable contribution to the application project as a member of the group, (2) read and fully agree with the contents (i.e., results, conclusions, analyses, simulations) of this document, and (3) acknowledged by name anyone outside this group who assisted this learning team or any individual member in the completion of this document.

Today’s date: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

Active members

1. \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_
2. \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_
3. \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

Acknowledgement of individual(s) who assisted this group in completing this document:

1. \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_
2. \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

**Abstract**

*Explain here the most significant developments, results or conclusions about the exercise. Use the remaining space in this sheet (200 words maximum).*

**Table of content**

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# Project specifications

## Specifications

The idea is to design a combinational system able to add and subtract 10-bit two’s complemented binary numbers. The circuit includes zero (Z), sign (S) and overflow indicators or flags (OV).

### Truth table

Normal text

### Example timing diagram

Normal text and reference to the Fig. 1.

Fig. 1 Example of a timing diagram showing several operations of the circuit.

## Theory

Explain whatever you consider important referring adding and subtracting binary numbers. For instance, this cross-reference ‎[4] is the Wikipedia entry for two’s complement (2C) numbers.

Fig. 2 This is an example of picture caption.

(Remember to reference all the copied and adapted materials from the web).

Consider using the Proteus circuit in P4 ‎[5] to try some input vectors.

Consider solving these operations below in 2C, so that you learn about the arithmetic and different results and flags’ values.

1. (+234) – (-133)
2. (-199) + (+216)
3. (-512) + (+511)
4. (+12 ) + (-511)
5. (+12 ) - (-511)

# Planning

## Hierarchical block diagram

This Fig. 3 is an example of picture representing a plan or a diagram. It can be scanned from an sketch in a sheet of paper.



Fig. 3 Example of hardware and software blocks involved in the design.

## Design phases

Which blocks or components are you going to design first?

# Development

Run EDA tools for synthesis specifying a target chip (FPGA or CPLD).

# Test and verification

Run EDA tools for simulation using a VHDL test bench.

## Functional simulation

Demonstrate using a logic analyser that the circuit works as expected.

## Gate-level simulation

Calculate and measure the maximum speed of computation/operation and discuss the results.

# Conclusions

Write a summary of the main features and conclusions of this project.

# References

Books.

1. Ercegovac, M., Lang, T., Moreno, J. H., Introduction to digital systems, John Wiley & Sons, 1999, John Wiley & Sons, 1999.This is the [book's web](http://web.cs.ucla.edu/Logic_Design/). Chapter 10 deals with [arithmetic circuits](http://web.cs.ucla.edu/Logic_Design/SLPDF/ch10.pdf).
2. (Add new books)

Web pages.

1. <http://digsys.upc.es>. This former ED unit [1.12](http://digsys.upc.es/ed/ED/unitats/unitat_1_12/Unitat_1_12.htm) contains descriptions of arithmetic circuits.
2. Two’s complement: <https://en.wikipedia.org/wiki/Two%27s_complement>
3. 8-bit two’s complement adder/subtractor solved in the Proteus simulator: <http://digsys.upc.es/csd/P03/Adder_subtractor_8bit.pdsprj>
4. (Add new web references)