Static Timing Analysis Techniques for FPGAs
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Why STA?

- Verify the design meets timing constraints
- Faster than timing-driven, gate-level simulation
- Ease design debugging
## Agenda

- Introduction to Static Timing Analysis
- Elements of Timing Verification
- Timing in FPGAs
- Analysis Examples
Overview

• Design Flow
• Dynamic Versus Static Simulation
• Key Definitions
  – Critical Path
  – Arrival Time
  – Required Time
  – Slack
# Dynamic Versus Static Verification

<table>
<thead>
<tr>
<th>Dynamic</th>
<th>Static</th>
</tr>
</thead>
<tbody>
<tr>
<td>Difficult to cover all paths</td>
<td>Checks every path for timing violations</td>
</tr>
<tr>
<td>Typically time and compute intensive</td>
<td>Typical runtime is fast</td>
</tr>
<tr>
<td>Confirms function and timing</td>
<td>Confirms timing only</td>
</tr>
<tr>
<td>Supports asynchronous designs</td>
<td>Synchronous designs only</td>
</tr>
<tr>
<td>Simple timing checks</td>
<td>Min/Max, clock skew, exceptions</td>
</tr>
<tr>
<td>Ex: Mentor Graphics ModelSim</td>
<td>Ex: Lattice Semiconductor trace program</td>
</tr>
</tbody>
</table>

## STA Compute Method

![STA Compute Method Diagram](image-url)
Timing Paths

Delay Calculation

- Intrinsic vs. Extrinsic Delay
- Logic Gate Delay
- Net Delay
- \( y = mx + b \)
Synchronous Circuit Delay Calculation

\[ T_{\text{propagation}} = T_{\text{period}} - T_{\text{setup}} \]

Path Measurements

<table>
<thead>
<tr>
<th>Path</th>
<th>Signal Route</th>
<th>Delay</th>
</tr>
</thead>
<tbody>
<tr>
<td>g2 to g8</td>
<td>g2(Tq) n3 g5 n6 g6 n6</td>
<td>12 + Tdq + Ts</td>
</tr>
<tr>
<td>g2 to g9</td>
<td>g2(Tq) n3 g5 n7 g7 n7</td>
<td>12 + Tdq + Ts</td>
</tr>
<tr>
<td>g4 to g8</td>
<td>g4(Tq) n4 g5 n6 g6 n8</td>
<td>12 + Tdq + Ts</td>
</tr>
</tbody>
</table>
Constraint Checks

• Min/Max Delay
• Setup/Hold
• Recovery/Removal
• Clock Definitions
  – Gated Clocks
  – Clock Skews and Multiple Clock Groups
  – Multi-frequency Clocks
  – Multi-phase Clocks
• False Paths
• Multi-cycle Path Analysis

Min/Max Delay

Path 4: primary input to primary output (Tpd)

================================================================================
Preference: MAXDELAY FROM PORT "in1" TO PORT "op1" 9.000000 ns ;
  1 item scored, 0 timing errors detected.
================================================================================
Logical Details:  Cell type  Pin type       Cell/ASIC name  (clock net +/-)
Source:         Port       Pad            in1
Destination:    Port       Pad            op1
Delay:               3.541ns  (63.2% logic, 36.8% route), 3 logic levels.
Constraint Details:
  3.541ns physical path delay in1 to op1 meets
  9.000000ns delay constraint by 5.459ns

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Setup/Hold Basics

Setup/Hold Checking for Flip-Flops
PCB Requirements for Setup/Hold

- Port Controller
- Lattice FPGA

- 9 pf input capacitance.
- 60 pf AC load
- 3 ns to 18 ns clk to out,
  5 ns setup, 3 ns hold

Lattice FPGA

- INPUT SETUP = P - (PDMAXp + PDMAXb + Tskew) = 15 - (9 + 3 + 0.5) = 15 - 12.5 = 2.5 ns
- HOLD = PDMINp + PDMINb - Tskew = 1.5 + 0.5 - 0.5 = 1.5 ns
- PERIOD PORT "clk" 15 ns ;
- INPUT_SETUP GROUP "ina" 2.5 ns HOLD 1.5 ns CLKPORT "clk" ;

I/O Setup Analysis Example

- Preference: INPUT_SETUP GROUP "ina" 2.500000 ns HOLD 1.500000 ns CLKPORT "clk" ; Setup Analysis.
- 16 items scored, 0 timing errors detected.

- Passed: The following path meets requirements by 2.582 ns.

Logical Details: Cell type Pin type Cell/ASIC name (clock net +/-)
Source: Port Pad ina(0)
Destination: FF Unknown GA_0 (to clk_int +)

Max Data Path Delay: 0.542 ns [100.0% logic, 0.0% route], 1 logic levels.
Min Clock Path Delay: 1.527 ns [30.2% logic, 69.8% route], 1 logic levels.

Constraint Details:
- 0.542 ns delay ina(0) to ina(0)_MGUI less 2.500 ns offset ina(0) to clk (totaling -1.958 ns) meets
  1.527 ns delay clk to ina(0)_MGUI less 0.903 ns DI_SET requirement (totaling 0.624 ns) by 2.582 ns.

Physical Path Details:
- Data path ina(0) to ina(0)_MGUI:
<table>
<thead>
<tr>
<th>Name</th>
<th>Fanout</th>
<th>Delay (ns)</th>
<th>Site</th>
<th>Resource</th>
</tr>
</thead>
<tbody>
<tr>
<td>PADI_DEL</td>
<td>0.542</td>
<td>32.PAD to 32.PADDI ina(0)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>ROUTE</td>
<td>2.000</td>
<td>32.PADDI to IOL_B8A.DI ina_int(0) (to clk_int)</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

- 0.542 ns [100.0% logic, 0.0% route], 1 logic levels.

- Clock path clk to ina(0)_MGUI:
<table>
<thead>
<tr>
<th>Name</th>
<th>Fanout</th>
<th>Delay (ns)</th>
<th>Site</th>
<th>Resource</th>
</tr>
</thead>
<tbody>
<tr>
<td>PADI_DEL</td>
<td>0.461</td>
<td>90.PAD to 90.PADDI clk</td>
<td></td>
<td></td>
</tr>
<tr>
<td>ROUTE</td>
<td>24.064</td>
<td>90.PADDI to IOL_B8A.CLK clk_int</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

- 1.527 ns [30.2% logic, 69.8% route], 1 logic levels.

Report: There is no minimum offset greater than zero for this preference.
I/O Hold Analysis Example

16 items scored, 16 timing errors detected.

Error: The following path exceeds requirements by 0.631ns

Logical Details: Cell type Pin type Cell/ASIC name (clock net +/-)
Source: Port Pad ina(0)
Destination: FF Unknown GA_0 (to clk_int +)
Min Data Path Delay: 0.461ns [100.0% logic, 0.0% route], 1 logic levels.
Max Clock Path Delay: 2.014ns [26.9% logic, 73.1% route], 1 logic levels.

Constraint Details:
0.461ns delay ina(0) to ina(0)_MGIOL plus
1.500ns hold offset ina(0) to clk (totaling 1.961ns) violates
2.014ns delay clk to ina(0)_MGIOL plus
0.578ns DI_HLD requirement (totaling 2.592ns) by 0.631ns

Physical Path Details:

<table>
<thead>
<tr>
<th>Name</th>
<th>Fanout</th>
<th>Delay (ns)</th>
<th>Site</th>
<th>Resource</th>
</tr>
</thead>
<tbody>
<tr>
<td>PADI_DEL</td>
<td>---</td>
<td>0.461</td>
<td>32.PAD to</td>
<td>32.PADDI ina(0)</td>
</tr>
<tr>
<td>ROUTE</td>
<td>2</td>
<td>0.000</td>
<td>32.PADDI to</td>
<td>IOL_B8A.DI ina_int(0) (to clk_int)</td>
</tr>
<tr>
<td>--------</td>
<td>-----</td>
<td>------</td>
<td>------------------</td>
<td>---------</td>
</tr>
<tr>
<td></td>
<td>0.461</td>
<td>100.0% logic, 0.0% route, 1 logic levels.</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Warning: 2.131ns is the minimum offset for this preference.

Hold Analysis Example

Preference: INPUT_SETUP GROUP "ina" 2.500000 ns HOLD 1.500000 ns CLEPORT "clk" ;
16 items scored, 0 timing errors detected.
Passed: The following path meets requirements by 1.669ns

Logical Details: Cell type Pin type Cell/ASIC name (clock net +/-)
Source: Port Pad ina(7)
Destination: FF Data in GA_7 (to pllclk +)
Min Data Path Delay: 0.436ns [44.7% logic, 55.3% route], 1 logic levels.
Max Clock Path Delay: 1.167ns [19.6% logic, 80.4% route], 2 logic levels.

Constraint Details:
0.436ns delay ina(7) to SLICE_3 plus
1.500ns hold offset ina(7) to clk (totaling 1.936ns) meets
1.167ns delay clk to SLICE_3 less
0.874ns feedback compensation less
-0.026ns M_HLD requirement (totaling 0.267ns) by 1.669ns

Physical Path Details:

Report: There is no minimum offset greater than zero for this preference.
Questions?

Clock Definitions

Tu = Clock uncertainty

Earliest rising edge

Latest rising edge
Polarity Skew

FF1clk

FF2clk

Td = Polarity skew

FF1

FF2

Polarity Skew Analysis Example

Preference: PERIOD PORT "clk" 3.000000 ns ;
32 items scored, 16 timing errors detected.

Error: The following path exceeds requirements by 0.379ns

Logical Details: Cell type Pin type Cell/ASIC name (clock net +/-)
Source: FF Q FF1_9_0io (from clk_c +)
Destination: FF Unknown FF2_9_0io (to clk_c -)
Delay: 1.896ns (31.1% logic, 68.9% route), 2 logic levels.

Constraint Details:
1.896ns physical path delay SLICE_4 to outa_9_MGIO exceeds
1.500ns delay constraint less
0.125ns skew and
-0.142ns ONEG0_SET requirement (totaling 1.517ns) by 0.379ns

Physical Path Details:
Name   Fanout   Delay (ns)   Site   Resource
REG_DEL   --- 0.354      R3C2D.CLK to R3C2D.Q1 SLICE_4 (from clk_c)
ROUTE    1 0.560      R3C2D.Q1 to R4C2D.C0 n2_9
CTOF_DEL  --- 0.235       R4C2D.C0 to R4C2D.F0 SLICE_14
ROUTE    1 0.747       R4C2D.F0 to IOL_L4A.ONEG0 n3_9 (to clk_c)
----------
1.896   (31.1% logic, 68.9% route), 2 logic levels.

Clock Skew Details:
Source Clock:
Delay  Connection
1.597ns  90.PADDI to R3C2D.CLK
Destination Clock:
Delay  Connection
1.472ns  90.PADDI to IOL_L4A.CLK

Warning: 3.758ns is the minimum period for this preference.
Phase Skew Analysis Example

Preference: FREQUENCY NET "FF1clk" 250.000000 MHz ;
16 items scored, 0 timing errors detected.
Passed: The following path meets requirements by 1.758ns
Logical Details: Cell type Pin type Cell/ASIC name (clock net +/-)
Source: FF Port Pad ina_9
Destination: FF Data in FF1_9 (to FF1clk +)
Delay: 2.129ns (25.5% logic, 74.5% route), 1 logic levels.
Constraint Details:
2.129ns physical path delay ina_9 to SLICE_4 meets
4.000ns delay constraint less
0.113ns M_SET requirement (totaling 3.887ns) by 1.758ns :

Preference: FREQUENCY NET "FF2clk" 250.000000 MHz ;
16 items scored, 0 timing errors detected.
Passed: The following path meets requirements by 2.249ns
and meets 4.000ns delay constraint requirement for source clock "FF1clk"
by 2.249ns
Logical Details: Cell type Pin type Cell/ASIC name (clock net +/-)
Source: FF Port Pad FF1_7 (from FF1clk +)
Destination: FF Unknown FF2_7_0io (to FF2clk +)
Delay: 2.323ns (25.4% logic, 74.5% route), 2 logic levels.
Constraint Details:
2.323ns physical path delay SLICE_3 to outa_7_MGIOL meets
4.000ns delay constraint less
-0.375ns skew and
-0.000ns feedback compensation and
-0.197ns ONEG0_SET requirement (totaling 4.572ns) by 2.249ns ;
Phase Skew Analysis Example

**Clock Skew Details:**

**Source Clock Path:**

<table>
<thead>
<tr>
<th>Name</th>
<th>Fanout</th>
<th>Delay (ns)</th>
<th>Site</th>
<th>Resource</th>
</tr>
</thead>
<tbody>
<tr>
<td>PADI_DEL</td>
<td>1</td>
<td>0.542</td>
<td>19.PAD to</td>
<td>19.PADDI pllclk</td>
</tr>
<tr>
<td>ROUTE</td>
<td>0.000</td>
<td>0.000</td>
<td>19.PADDI to PLL3_R6C1.CLKI to</td>
<td>PLL3_R6C1.CLKI pllclk_c</td>
</tr>
<tr>
<td>CLK2007_DEL</td>
<td>9</td>
<td>1.874</td>
<td>LL3_R6C1.CLK to</td>
<td>I1/PLLBInst_0</td>
</tr>
<tr>
<td>ROUTE</td>
<td>0.000</td>
<td>0.000</td>
<td>LL3_R6C1.CLK to</td>
<td>R14C14B.CLK FF1clk</td>
</tr>
</tbody>
</table>

**Destination Clock Path:**

<table>
<thead>
<tr>
<th>Name</th>
<th>Fanout</th>
<th>Delay (ns)</th>
<th>Site</th>
<th>Resource</th>
</tr>
</thead>
<tbody>
<tr>
<td>PADI_DEL</td>
<td>1</td>
<td>0.542</td>
<td>19.PAD to</td>
<td>19.PADDI pllclk</td>
</tr>
<tr>
<td>ROUTE</td>
<td>0.000</td>
<td>0.000</td>
<td>19.PADDI to PLL3_R6C1.CLKI to</td>
<td>PLL3_R6C1.CLKI pllclk_c</td>
</tr>
<tr>
<td>CLK2P_DEL</td>
<td>16</td>
<td>1.749</td>
<td>LL3_R6C1.CLKOS to</td>
<td>I1/PLLBInst_0</td>
</tr>
</tbody>
</table>

---

2.416 (22.4% logic, 77.6% route), 2 logic levels.

PLL3_R6C1.CLKOS attributes: FDEL = 0

---

2.791 (37.3% logic, 62.7% route), 2 logic levels.

PLL3_R6C1.CLKOS attributes: PHASEADJ = 45, FDEL = 0

**Source Clock f/b:**

<table>
<thead>
<tr>
<th>Name</th>
<th>Fanout</th>
<th>Delay (ns)</th>
<th>Site</th>
<th>Resource</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLKOP_DEL</td>
<td>9</td>
<td>1.749</td>
<td>LL3_R6C1.CLKFB to</td>
<td>LL3_R6C1.CLKOP FF1clk</td>
</tr>
</tbody>
</table>

---

1.749 (0% logic, 100% route), 1 logic levels.

PLL3_R6C1.CLKOP attributes: FDEL = 0

**Destination Clock f/b:**

<table>
<thead>
<tr>
<th>Name</th>
<th>Fanout</th>
<th>Delay (ns)</th>
<th>Site</th>
<th>Resource</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLKOP_DEL</td>
<td>9</td>
<td>1.749</td>
<td>LL3_R6C1.CLKFB to</td>
<td>LL3_R6C1.CLKOP FF1clk</td>
</tr>
</tbody>
</table>

---

1.749 (0% logic, 100% route), 1 logic levels.

PLL3_R6C1.CLKOP attributes: FDEL = 0

---

**Frequency Skew**

![Frequency Skew Diagram](image-url)
Frequency Skew Analysis Example

Preference: PERIOD PORT "FF1clk" 4.500000 nS;
16 items scored, 0 timing errors detected.
Passed: The following path meets requirements by 2.745ns
Logical Details: Cell type Pin type Cell/ASIC name (clock net +/-)
Source: Port Pad ina(6)
Destination: FF Data in FF1_6 (to FF1clk_int +)
Delay: 1.642ns (33.0% logic, 67.0% route), 1 logic levels.
Constraint Details:
1.642ns physical path delay ina(6) to SLICE_3 meets
4.500ns delay constraint less
0.113ns M_SET requirement (totaling 4.387ns) by 2.745ns
Report: 1.755ns is the minimum period for this preference.

Preference: PERIOD PORT "FF2clk" 2.000000 nS;
16 items scored, 0 timing errors detected.
WARNING - trce: Clock skew between net 'FF1clk_int' and net 'FF2clk_int' not computed:
nets may not be related
Passed: The following path meets requirements by 0.158ns and meets
4.500ns delay constraint requirement for source clock "FF1clk_int" by 2.658ns
Logical Details: Cell type Pin type Cell/ASIC name (clock net +/-)
Source: FF Q FF1_12 (from FF1clk_int +)
Destination: FF Unknown FF2_12 (to FF2clk_int +)
Delay: 2.039ns (28.9% logic, 71.1% route), 2 logic levels.
Constraint Details:
2.039ns physical path delay SLICE_6 to outa(12)_MGIOL meets
2.000ns delay constraint less
-0.197ns ONEG0_SET requirement (totaling 2.197ns) by 0.158ns
Report: 1.842ns is the minimum period for this preference.

ModelSim
Design Planner
Lattice Semiconductor Corporation
Bringing the Best Together
Cycle Skew Analysis Example

Preference: `PERIOD PORT "clk" 3.000000 ns`;
32 items scored, 1 timing error detected.
Error: The following path exceeds requirements by 0.133ns:
Constraint Details:
- 3.330ns physical path delay sel to outa_15_MGIOL exceeds
- 3.000ns delay constraint less
- -0.197ns ONEG0_SET requirement (totaling 3.197ns) by 0.133ns.

Preference: `MULTICYCLE FROM GROUP "FF1" TO GROUP "FF2" 2.000000 X`;
16 items scored, 0 timing errors detected.
Passed: The following path meets requirements by 3.491ns.
Logical Details: Cell type Pin type Cell/ASIC name (clock net +/-)
Source: FF Q FF1_10 (from clk_c +)
Destination: FF Unknown FF2_10_0io (to clk_c +)
Delay: 2.581ns (22.8% logic, 77.2% route), 2 logic levels.
Constraint Details:
- 2.581ns physical path delay SLICE_5 to outa_10_MGIOL meets
- 6.000ns delay constraint less
- 0.125ns skew and
- -0.197ns ONEG0_SET requirement (totaling 6.072ns) by 3.491ns.
False Paths

Analysis of Phase-Locked Loops
Timing Analysis By Stage

• Preliminary Timing Analysis
• Synthesis Timing Analysis
  – RTL vs. Gate-Level
  – Timing in RTL Code
  – Black-Box Timing Arcs
• Place & Route Timing Analysis
  – Post-Map
  – Post-Placement
  – Post-Route

Timing Parameters

• Corners and STA
• Timing Derating Factors
• Grading FPGAs by Speed
• Best-Case Delay Values
Synthesis STA with Precision

- Timing Specification
  - Native or Synopsys (SDC) Format
- Analysis Commands
- Timing Report

Synthesis STA with Synplify

- Timing Specification
  - Native Synplify Design Constraints
- Analysis Commands
- Timing Report
Place & Route STA with ispLEVER

- STA Setup, Project Navigator
- TRACE Report
- Routing Congestion with Design Planner
- Viewing Critical Paths with Design Planner
- I/O Timing Report

Summary

- Leverage STA engines throughout flow
- Handle fundamentals: clocks and I/O timing
- Advanced constraints for multicycle and blocks
- Simulate or formal methods for clock domain crossing
Resources

- Actel, Static Timing Analysis Using Designer’s Timer, Application Note. January 2004
- Lattice Semiconductor, ispLEVER FPGA Design Guide. 2006
- Lattice Semiconductor, LatticeEC FPGA Design with ispLEVER Tutorial. 2006
- Nekoogar, *Timing Verification of Application-Specific Integrated Circuits (ASICs)*, Prentice Hall PTR, 1999
- Xilinx, Development System Reference Guide, 2005

Thank You!

Interested in learning more ……..

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Questions?