74F160A • 74F162A
Synchronous Presettable BCD Decade Counter

General Description
The 74F160A and 74F162A are high-speed synchronous decade counters operating in the BCD (8421) sequence. They are synchronously presettable for applications in programmable dividers. There are two types of Count Enable inputs plus a Terminal Count output for versatility in forming synchronous multistage counters. The F160A has an asynchronous Master Reset input that overrides all other inputs and forces the outputs LOW. The F162A has a Synchronous Reset input that overrides counting and parallel loading and allows all outputs to be simultaneously reset on the rising edge of the clock. The F160A and F162A are high speed versions of the F160 and F162.

Features
- Synchronous counting and loading
- High-speed synchronous expansion
- Typical count rate of 120 MHz

Ordering Code:

<table>
<thead>
<tr>
<th>Order Number</th>
<th>Package Number</th>
<th>Package Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>74F160ASC</td>
<td>M16A</td>
<td>16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow</td>
</tr>
<tr>
<td>74F160ASJ</td>
<td>M16D</td>
<td>16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide</td>
</tr>
<tr>
<td>74F160APC</td>
<td>N16E</td>
<td>16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide</td>
</tr>
<tr>
<td>74F162ASC</td>
<td>M16A</td>
<td>16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow</td>
</tr>
<tr>
<td>74F162APC</td>
<td>N16E</td>
<td>16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide</td>
</tr>
</tbody>
</table>

Connection Diagrams

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### Logic Symbols

#### Unit Loading/Fan Out

<table>
<thead>
<tr>
<th>Pin Names</th>
<th>Description</th>
<th>U.L. HIGH/LOW</th>
<th>Input $I_{HW}/I_{IL}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>CEP</td>
<td>Count Enable Parallel Input</td>
<td>1.0/1.0</td>
<td>20 µA/−0.6 mA</td>
</tr>
<tr>
<td>CET</td>
<td>Count Enable Trickle Input</td>
<td>1.0/2.0</td>
<td>20 µA/−1.2 mA</td>
</tr>
<tr>
<td>CP</td>
<td>Clock Pulse Input (Active Rising Edge)</td>
<td>1.0/1.0</td>
<td>20 µA/−0.6 mA</td>
</tr>
<tr>
<td>MR (74F160A)</td>
<td>Asynchronous Master Reset Input (Active LOW)</td>
<td>1.0/1.0</td>
<td>20 µA/−0.6 mA</td>
</tr>
<tr>
<td>SR (74F162A)</td>
<td>Synchronous Reset Input (Active LOW)</td>
<td>1.0/2.0</td>
<td>20 µA/−1.2 mA</td>
</tr>
<tr>
<td>$P_0$-$P_3$</td>
<td>Parallel Data Inputs</td>
<td>1.0/1.0</td>
<td>20 µA/−0.6 mA</td>
</tr>
<tr>
<td>PE</td>
<td>Parallel Enable Input (Active LOW)</td>
<td>1.0/2.0</td>
<td>20 µA/−1.2 mA</td>
</tr>
<tr>
<td>$Q_0$-$Q_3$</td>
<td>Flip-Flop Outputs</td>
<td>50/33.3</td>
<td>−1 mA/20 mA</td>
</tr>
<tr>
<td>TC</td>
<td>Terminal Count Output</td>
<td>50/33.3</td>
<td>−1 mA/20 mA</td>
</tr>
</tbody>
</table>
Functional Description

The 74F160A and 74F162A count modulo-10 in the BCD (8421) sequence. From state 9 (HLLH) they increment to state 0 (LLLL). The clock inputs of all flip-flops are driven in parallel through a clock buffer. Thus all changes of the Q outputs (except due to Master Reset of the (F160A) occur as a result of, and synchronous with, the LOW-to-HIGH transition of the CP input signal. The circuits have four fundamental modes of operation, in order of precedence: asynchronous reset (F160A), synchronous reset (F162A), parallel load, count-up and hold. Five control inputs—Master Reset (MR, F160A), Synchronous Reset (SR, F162A), Parallel Enable (PE), Count Enable Parallel (CEP) and Count Enable Trickle (CET)—determine the mode of operation, as shown in the Mode Select Table. A LOW signal on MR overrides all other inputs and asynchronously forces all outputs LOW. A LOW signal on SR overrides counting and parallel loading and allows all outputs to go LOW on the next rising edge of CP. A LOW signal on PE overrides counting and allows information on the Parallel Data (P_n) inputs to be loaded into the flip-flops on the next rising edge of CP. With PE and MR (F160A) or SR (F162A) HIGH, CEP and CET permit counting when both are HIGH. Conversely, a LOW signal on either CEP or CET inhibits counting.

Mode Select Table

<table>
<thead>
<tr>
<th>SR</th>
<th>PE</th>
<th>CET</th>
<th>CEP</th>
<th>Action on the Rising Clock Edge (→)</th>
</tr>
</thead>
<tbody>
<tr>
<td>L</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>Reset (Clear)</td>
</tr>
<tr>
<td>H</td>
<td>L</td>
<td>X</td>
<td>X</td>
<td>Load (P_n → Q_n)</td>
</tr>
<tr>
<td>H</td>
<td>H</td>
<td>H</td>
<td>H</td>
<td>Count (Increment)</td>
</tr>
<tr>
<td>H</td>
<td>H</td>
<td>L</td>
<td>X</td>
<td>No Change (Hold)</td>
</tr>
<tr>
<td>H</td>
<td>H</td>
<td>L</td>
<td>L</td>
<td>No Change (Hold)</td>
</tr>
</tbody>
</table>

*For 74F162A only
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Logic Equations:

Count Enable = CEP × CET × PE
TC = Q_0 × Q_1 × Q_2 × Q_3 × CET

State Diagram

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.
Absolute Maximum Ratings (Note 1)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Storage Temperature</td>
<td>−65°C to +150°C</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Ambient Temperature under Bias</td>
<td>−55°C to +125°C</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Junction Temperature under Bias</td>
<td>−55°C to +150°C</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VCC Pin Potential to Ground Pin</td>
<td>−0.5V to +7.0V</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Voltage (Note 2)</td>
<td>−0.5V to +7.0V</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Current (Note 2)</td>
<td>−30 mA to +5.0 mA</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Voltage Applied to Output in HIGH State (with VCC = 0V)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Standard Output</td>
<td>−0.5V to VCC</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3-STATE Output</td>
<td>−0.5V to +5.5V</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Current Applied to Output in LOW State (Max)</td>
<td>twice the rated IOL (mA)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ESD Last Passing Voltage (Min)</td>
<td>4000V</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Recommended Operating Conditions

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Free Air Ambient Temperature</td>
<td>0°C to +70°C</td>
</tr>
<tr>
<td>Supply Voltage</td>
<td>+4.5V to +5.5V</td>
</tr>
</tbody>
</table>

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIH</td>
<td>Input HIGH Voltage</td>
<td>2.0</td>
<td></td>
<td>V</td>
<td>Recognized as a HIGH Signal</td>
<td></td>
</tr>
<tr>
<td>VIL</td>
<td>Input LOW Voltage</td>
<td>0.8</td>
<td></td>
<td>V</td>
<td>Recognized as a LOW Signal</td>
<td></td>
</tr>
<tr>
<td>VCD</td>
<td>Input Clamp Diode Voltage</td>
<td>−1.2</td>
<td></td>
<td>V</td>
<td>Min IIN = −18 mA</td>
<td></td>
</tr>
<tr>
<td>VOH</td>
<td>Output HIGH Voltage</td>
<td>2.5</td>
<td></td>
<td>V</td>
<td>Min ICH = +1 mA</td>
<td></td>
</tr>
<tr>
<td>VOH</td>
<td>Voltage</td>
<td>2.7</td>
<td></td>
<td>V</td>
<td>Min ICH = +1 mA</td>
<td></td>
</tr>
<tr>
<td>VIL</td>
<td>Output LOW Voltage</td>
<td>0.5</td>
<td></td>
<td>V</td>
<td>Min IOL = 20 mA</td>
<td></td>
</tr>
<tr>
<td>IH</td>
<td>Input HIGH Current</td>
<td>5.0</td>
<td></td>
<td>µA</td>
<td>Max VIN = 2.7V</td>
<td></td>
</tr>
<tr>
<td>IBIH</td>
<td>Input HIGH Current Breakdown Test</td>
<td>7.0</td>
<td></td>
<td>µA</td>
<td>Max VIN = 7.9V</td>
<td></td>
</tr>
<tr>
<td>IOEX</td>
<td>Output HIGH Leakage Current</td>
<td>50</td>
<td></td>
<td>µA</td>
<td>Max VOUT = VCC</td>
<td></td>
</tr>
<tr>
<td>IQD</td>
<td>Input Leakage Test</td>
<td>4.75</td>
<td></td>
<td>V</td>
<td>0.0</td>
<td>IQD = 1.9 µA All Other Pins Grounded</td>
</tr>
<tr>
<td>IOCD</td>
<td>Output Leakage Circuit Current</td>
<td>3.75</td>
<td></td>
<td>µA</td>
<td>0.0</td>
<td>VCC = 150 mV All Other Pins Grounded</td>
</tr>
<tr>
<td>LIL</td>
<td>Input LOW Current</td>
<td>−0.6</td>
<td></td>
<td>mA</td>
<td>Max VIN = −0.5V (CP, CE, PE, PEF (F160A))</td>
<td></td>
</tr>
<tr>
<td>LIL</td>
<td>Current</td>
<td>−1.2</td>
<td></td>
<td>mA</td>
<td>Max VIN = −0.5V (CE, SR, F162A, PE)</td>
<td></td>
</tr>
<tr>
<td>IOD</td>
<td>Output Short-Circuit Current</td>
<td>−60</td>
<td></td>
<td>−150 mA</td>
<td>Max VCC = 0V</td>
<td></td>
</tr>
<tr>
<td>ICC</td>
<td>Power Supply Current</td>
<td>37</td>
<td>55</td>
<td>mA</td>
<td>Max VO = HIGH</td>
<td></td>
</tr>
</tbody>
</table>
### AC Electrical Characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>( T_A = -25°C )</th>
<th>( T_A = -55°C ) to ( +125°C )</th>
<th>( T_A = 0°C ) to ( +70°C )</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>( V_{CC} = +5.0V )</td>
<td>( V_{CC} = +5.0V )</td>
<td>( V_{CC} = +5.0V )</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( C_L = 50 , \text{pF} )</td>
<td>( C_L = 50 , \text{pF} )</td>
<td>( C_L = 50 , \text{pF} )</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Min</td>
<td>Typ</td>
<td>Max</td>
</tr>
<tr>
<td>( t_{MAX} )</td>
<td>Maximum Count Frequency</td>
<td>90</td>
<td>120</td>
<td>75</td>
</tr>
<tr>
<td>( t_{PLH} )</td>
<td>Propagation Delay, Count CP to ( Q_n ) (PE Input HIGH)</td>
<td>3.5</td>
<td>5.5</td>
<td>7.5</td>
</tr>
<tr>
<td>( t_{PHL} )</td>
<td>Propagation Delay, Load CP to ( Q_n ) (PE Input LOW)</td>
<td>4.0</td>
<td>6.0</td>
<td>8.5</td>
</tr>
<tr>
<td>( t_{PLH} )</td>
<td>Propagation Delay CP to TC</td>
<td>5.0</td>
<td>10.0</td>
<td>14.0</td>
</tr>
<tr>
<td>( t_{PHL} )</td>
<td>Propagation Delay CET to TC</td>
<td>2.5</td>
<td>4.5</td>
<td>7.5</td>
</tr>
<tr>
<td>( t_{PLH} )</td>
<td>Propagation Delay MR to ( Q_n ) (74F160A)</td>
<td>5.5</td>
<td>9.0</td>
<td>12.0</td>
</tr>
<tr>
<td>( t_{PHL} )</td>
<td>Propagation Delay MR to TC (74F160A)</td>
<td>4.5</td>
<td>8.0</td>
<td>12.5</td>
</tr>
</tbody>
</table>

### AC Operating Requirements

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>( T_A = -25°C )</th>
<th>( T_A = -55°C ) to ( +125°C )</th>
<th>( T_A = 0°C ) to ( +70°C )</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>( V_{CC} = +5.0V )</td>
<td>( V_{CC} = +5.0V )</td>
<td>( V_{CC} = +5.0V )</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( C_L = 50 , \text{pF} )</td>
<td>( C_L = 50 , \text{pF} )</td>
<td>( C_L = 50 , \text{pF} )</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Min</td>
<td>Typ</td>
<td>Max</td>
</tr>
<tr>
<td>( t_s(H) )</td>
<td>Setup Time, HIGH or LOW ( P_n ) to CP (74F160A)</td>
<td>4.0</td>
<td>5.5</td>
<td>4.0</td>
</tr>
<tr>
<td>( t_s(L) )</td>
<td>Setup Time, HIGH or LOW ( P_n ) to CP (74F162A)</td>
<td>5.0</td>
<td>5.5</td>
<td>5.0</td>
</tr>
<tr>
<td>( t_H(H) )</td>
<td>Hold Time, HIGH or LOW ( P_n ) to CP</td>
<td>2.0</td>
<td>2.5</td>
<td>2.0</td>
</tr>
<tr>
<td>( t_H(L) )</td>
<td>Hold Time, HIGH or LOW ( P_n ) to CP</td>
<td>11.0</td>
<td>13.5</td>
<td>11.5</td>
</tr>
<tr>
<td>( t_s(H) )</td>
<td>Setup Time, HIGH or LOW ( P_n ) to CP (74F160A)</td>
<td>11.0</td>
<td>13.0</td>
<td>11.5</td>
</tr>
<tr>
<td>( t_s(L) )</td>
<td>Setup Time, HIGH or LOW ( P_n ) to CP (74F162A)</td>
<td>5.0</td>
<td>6.0</td>
<td>5.0</td>
</tr>
<tr>
<td>( t_H(H) )</td>
<td>Hold Time, HIGH or LOW ( P_n ) to CP</td>
<td>0.0</td>
<td>0.0</td>
<td>0.0</td>
</tr>
<tr>
<td>( t_H(L) )</td>
<td>Hold Time, HIGH or LOW ( P_n ) to CP</td>
<td>0.0</td>
<td>0.0</td>
<td>0.0</td>
</tr>
<tr>
<td>( t_s(H) )</td>
<td>Setup Time, HIGH or LOW ( CEP ) or ( CET ) to ( CP )</td>
<td>11.0</td>
<td>13.0</td>
<td>11.5</td>
</tr>
<tr>
<td>( t_s(L) )</td>
<td>Setup Time, HIGH or LOW ( CEP ) or ( CET ) to ( CP )</td>
<td>5.0</td>
<td>6.0</td>
<td>5.0</td>
</tr>
<tr>
<td>( t_H(H) )</td>
<td>Hold Time, HIGH or LOW ( CEP ) or ( CET ) to ( CP )</td>
<td>0.0</td>
<td>0.0</td>
<td>0.0</td>
</tr>
<tr>
<td>( t_H(L) )</td>
<td>Hold Time, HIGH or LOW ( CEP ) or ( CET ) to ( CP )</td>
<td>0.0</td>
<td>0.0</td>
<td>0.0</td>
</tr>
<tr>
<td>( t_W(H) )</td>
<td>Clock Pulse Width (Lead) ( \text{HIGH} ) or ( \text{LOW} )</td>
<td>5.0</td>
<td>5.0</td>
<td>5.0</td>
</tr>
<tr>
<td>( t_W(L) )</td>
<td>Clock Pulse Width (Count) ( \text{HIGH} ) or ( \text{LOW} )</td>
<td>4.0</td>
<td>5.0</td>
<td>4.0</td>
</tr>
<tr>
<td>( t_p(L) )</td>
<td>( \text{MR} ) Pulse Width, LOW (74F160A)</td>
<td>6.0</td>
<td>5.0</td>
<td>5.0</td>
</tr>
<tr>
<td>( t_{REC} )</td>
<td>Recovery Time ( \text{MR} ) to ( CP ) (74F160A)</td>
<td>6.0</td>
<td>6.0</td>
<td>6.0</td>
</tr>
</tbody>
</table>
Physical Dimensions inches (millimeters) unless otherwise noted

16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
Package Number M16A
Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M16D

NOTES:
A. CONFORMS TO EIAJ ED11-7220 REGISTRATION, ESTABLISHED IN DECEMBER, 1988.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS ARE EXCLUSIVE OF BUHRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
M16DRvB1

DIMENSIONS ARE IN MILLIMETERS

SEATING PLANE
0.60 ±0.15
1.25
0°-8° TYP
GAGE PLANE
0.35
7° TYP
0.15-0.25

LAND PATTERN RECOMMENDATION
16 15 10 9
1.27 TYP
5.01 TYP
9.27 TYP

(2.13 TYP)

ALL LEAD TIPS
2.1 MAX
1.8 ±0.1
0.15 ±0.05

0.17 ±0.01
0.05 ±0.01

1.27 TYP

ALL LEAD TIPS
0.47 TYP
10.2 ±0.1

3.9
3.5
2.1 ±0.1

PIN #1 IDENT.
Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Ident</th>
<th>0.136 ± 0.005</th>
<th>0.125 ± 0.150</th>
<th>0.030 ± 0.005</th>
<th>0.093 (2.286)</th>
<th>0.093</th>
<th>0.250 ± 0.010</th>
<th>0.060 (1.524)</th>
<th>0.060</th>
<th>0.09 (2.54)</th>
<th>0.008 ± 0.016</th>
<th>0.045 (1.15)</th>
<th>0.045</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td>8</td>
<td>(3.402 ± 0.127)</td>
<td>(3.175 ± 0.381)</td>
<td>(1.270 ± 0.254)</td>
<td>(8.350 ± 0.254)</td>
<td>2</td>
<td>(7.420 ± 0.128)</td>
<td>(7.112)</td>
<td>0.280</td>
<td>(0.711)</td>
<td>(8.255 ± 0.38)</td>
<td>0.065</td>
<td></td>
</tr>
</tbody>
</table>

16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
Package Number N16E

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LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.

2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.